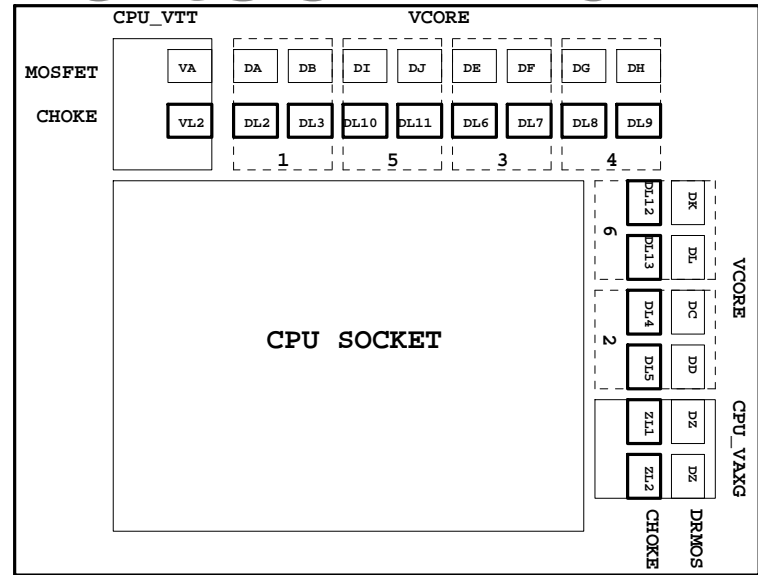


Model Name: GA-Z77X-UD5H(-WB) rev 1.03

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*16/*8/*4 SWITCH
18	PCI EXPRESS*1 SLOTS X3
19	ITE 8892
20	PCI SLOT 1
21	HDMI / DVI / DP
22	MSATA
23	Dual BIOS
24	ALC898
25	REAR AUDIO JACK
26	AMPLIFIER
27	PWM_IR 3567
28	VCORE POWER
29	VAXG POWER
30	PWM_IR 3570
31	VTT & DDR POWER
32	DISCRETE POWER I

SHEET	TITLE
33	VCCSA POWER
34	I/O ITE8728
35	F_PANEL , F_USB , PHOT
36	F_USB3.0
37	ATX POWER, CLOCK GEN
38	HWM,KB/MS , FAN CTRL
39	ARTHEROS AR8161/AR8151
40	INTEL 82579V
41	Marvell 9172(F+R)
42	Marvell 9172(F)
43	VT6308P 1394
44	VL810 USB3_HUB1(R)
45	VL810 USB3_HUB1(F)
46	RST, PWR, CLR_CMOS
47	TABLE LIST
48	



GA-Z77X-UD5H(-WB)

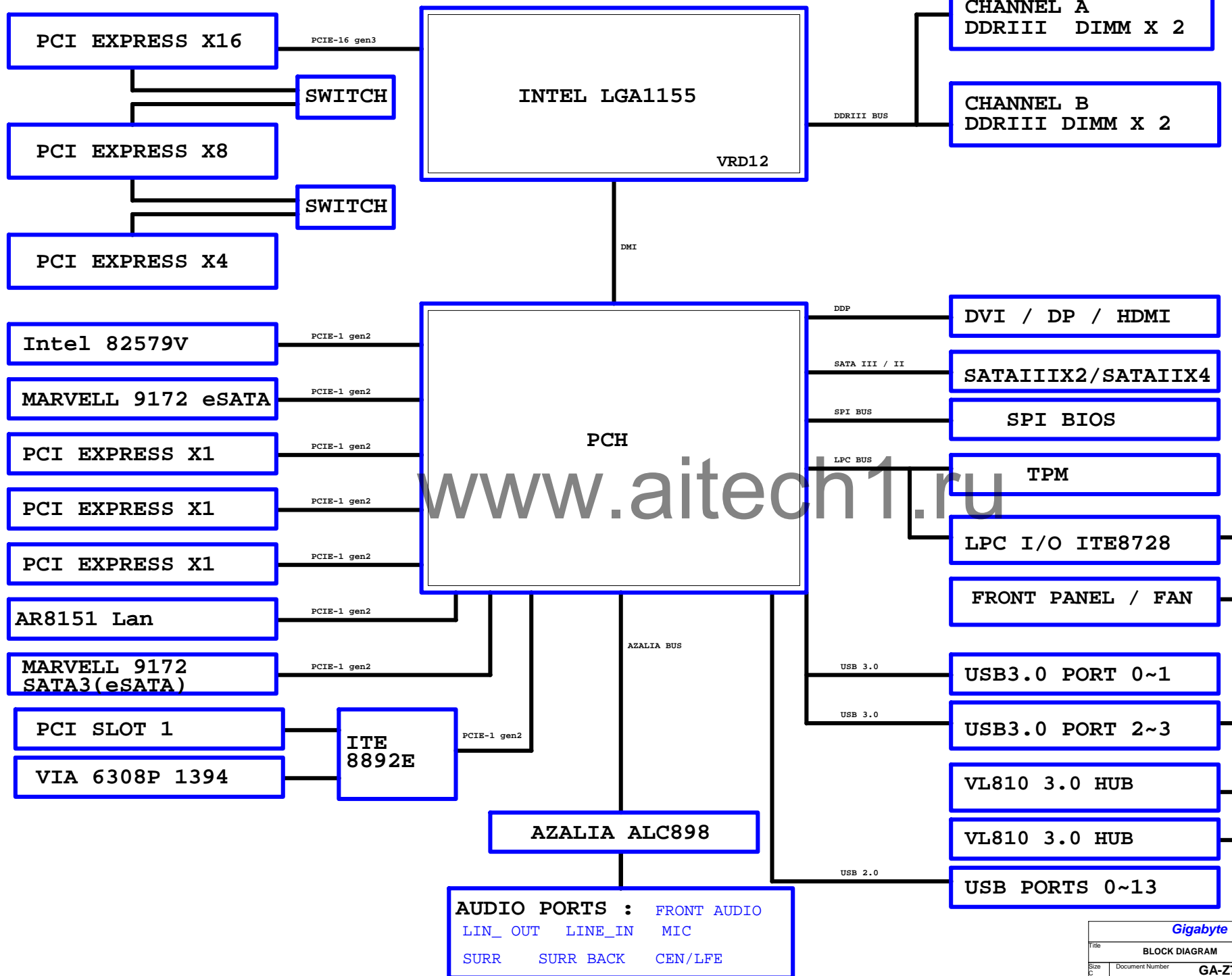
Component value change history

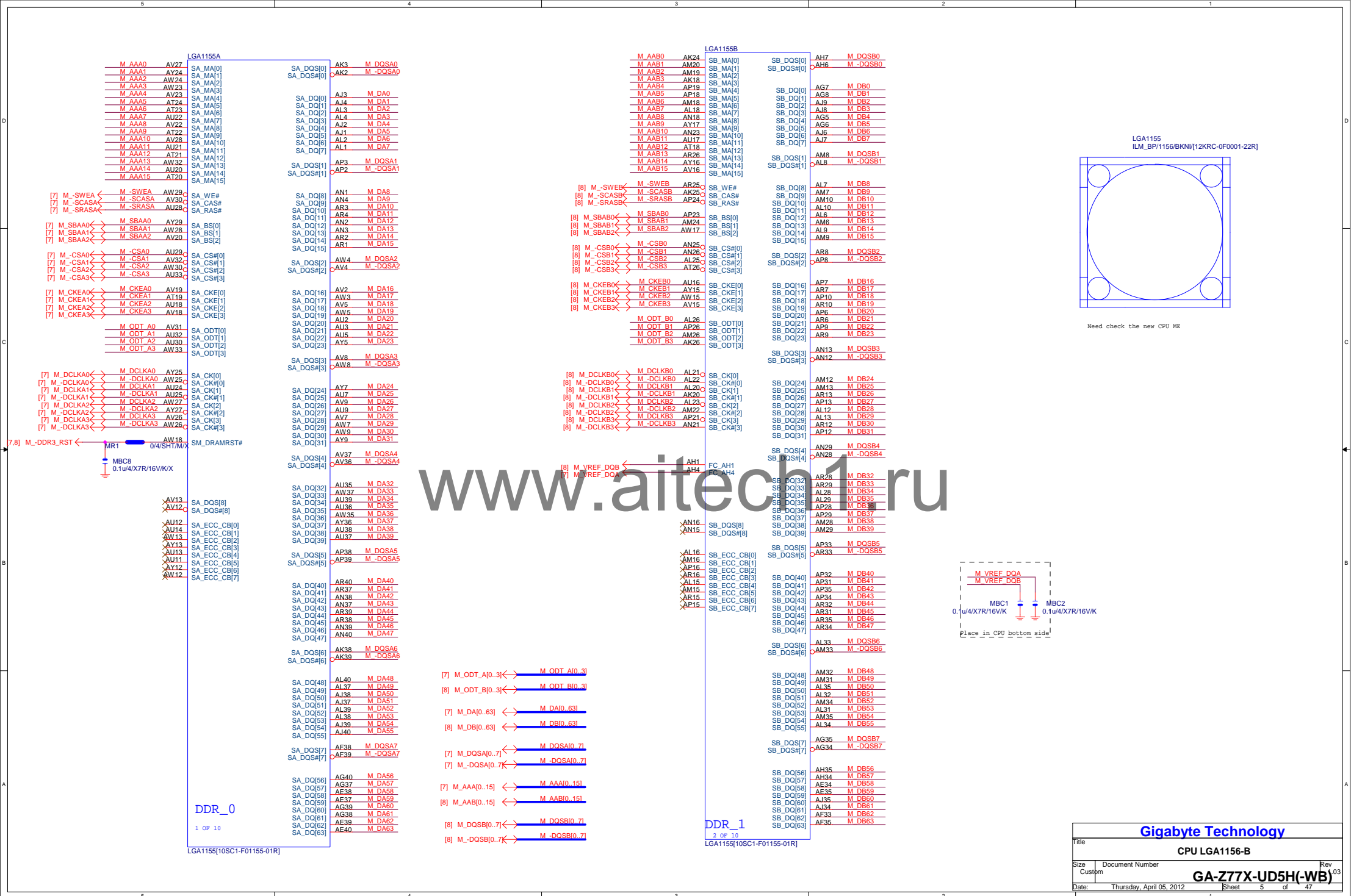
Data	Change Item	Reason
2011/02/10	0.2A	
	REMOVE AMplifier _ISL54405	
2012/01/03	1.0A-EBOM	
	vcore 改 上1下2	
	IT8892改FX	
	Vcore, VTT, vaxg circuit modify =>remove 3931	
2012/01/18	1.0	
	修改值for Magntiude Response高频高於-1dB	
	改+12v driver piull high R=>0ohm	
	Q41=>MODIFY : SIR840DP/N/5.4m/PPAKSO-8/[10IF9-040393-01R] for on/off charge	
2012/01/19	1.01B	
	修改 PCB 文字面 "SYS_FAN 1", "SYS_FAN 2", "SYS_FAN 3""SYS_FAN 4"	
2012/01/30	1.01C	
	改PROCHOT 阻值	
	改driver串0 ohm to 5v	
	改choke : 0.36uH/38A/IGC109/FS/D/[11LC5-F3360B-01R]	
2012/02/03	1.01D	
	FOR Vcore and Vaxg bom modify	
	For dvi test add HR83	
2012/03/05	1.01E	
	ADD HR147 HR148 FOR VIA HUB USB3 LOSS ISSUE ;	
	ADD MB_ID2 ; H : VIA HUB reset L : 1.01	
2012/03/06	1.02J	
	ADD CPU CFG9 CTRIL	
	ADD DBC126 for EMI	
	ADD MB_ID3 H:Rev1.02	
	ADD MR14,MBC34,MBC35,MBC36,MR15	
2012/03/22	1.03K	
	Modify PCB	

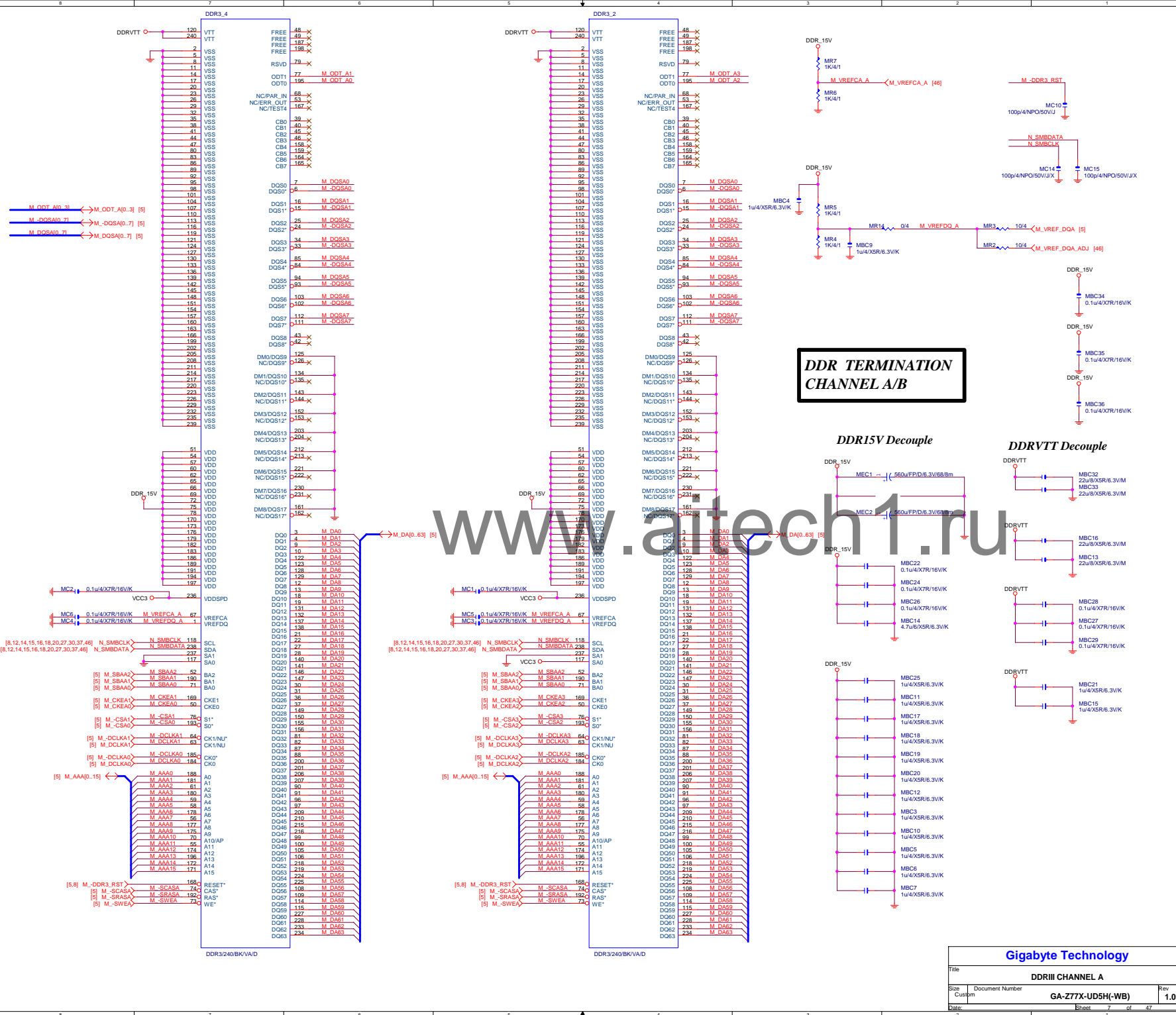
Circuit or PCB layout change

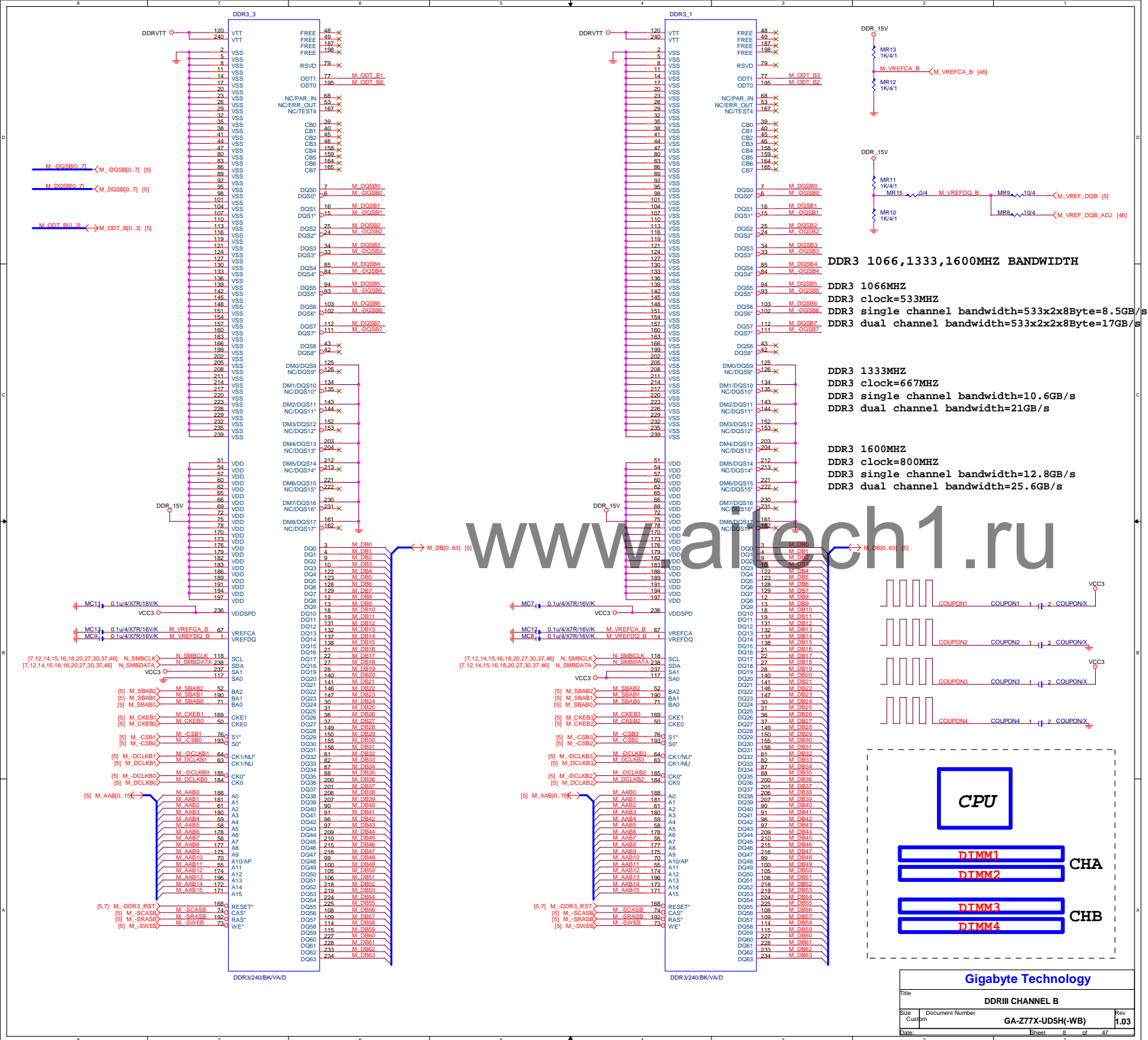
DATE	Change Item	Reason
2012/01/19	REV1.01 修改 PCB 文字面 "SYS_FAN 1", "SYS_FAN 2", "SYS_FAN 3""SYS_FAN 4"	
2012/03/02	REV1.02 修改DDR部分	
2012/03/21	REV1.03 修改文字面	

BLOCK DIAGRAM



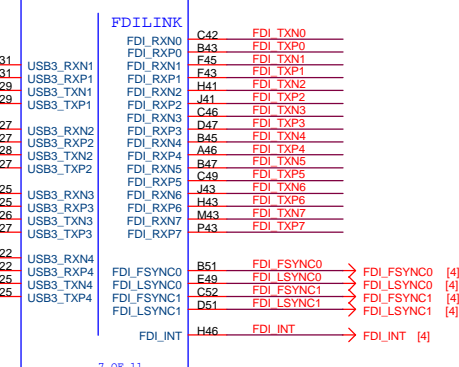
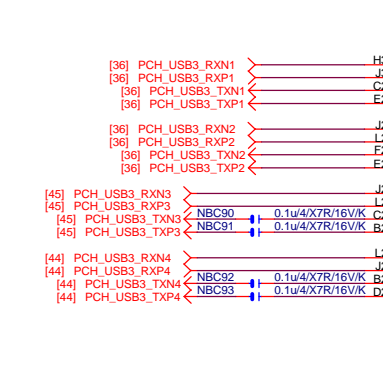
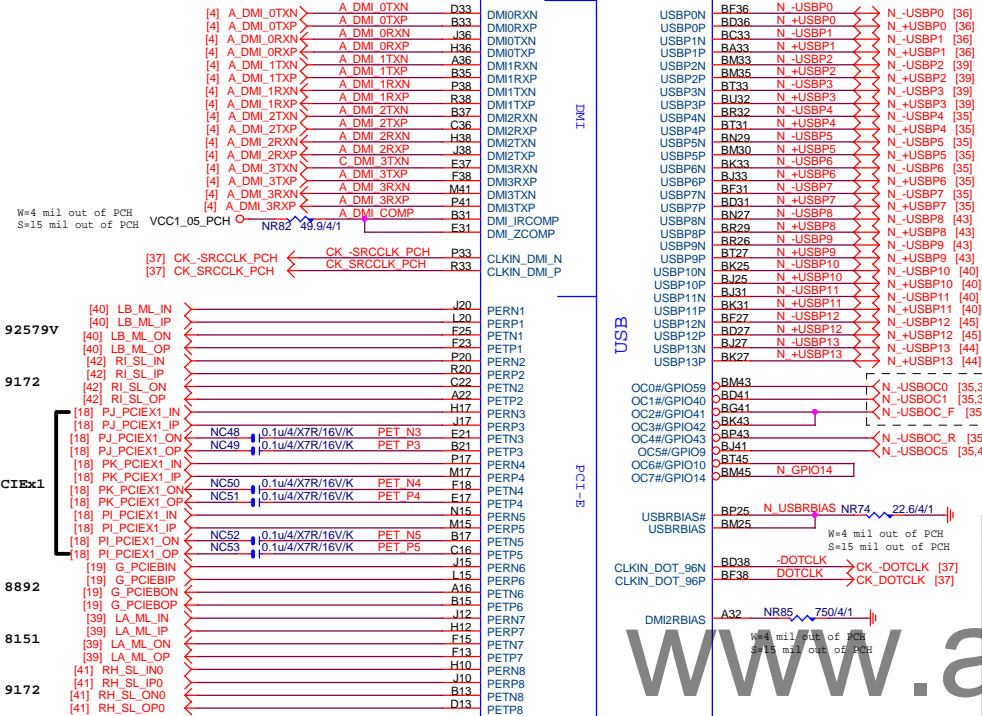






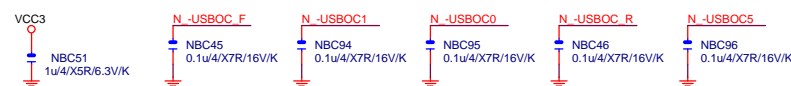
PCBH USB:12/7.5/4.5/7.5/12 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

PCHG



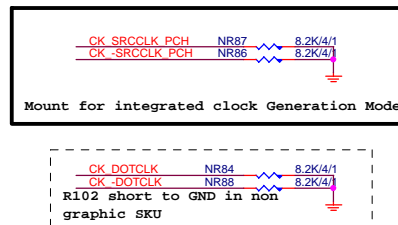
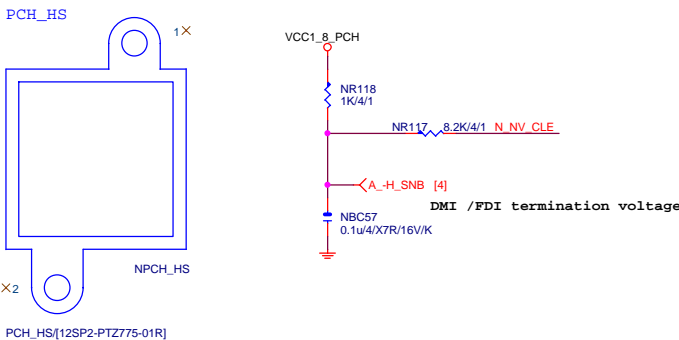
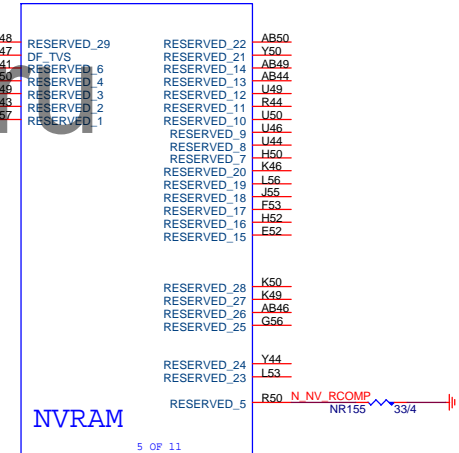
PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)
Impedance=80 +- 17.5%

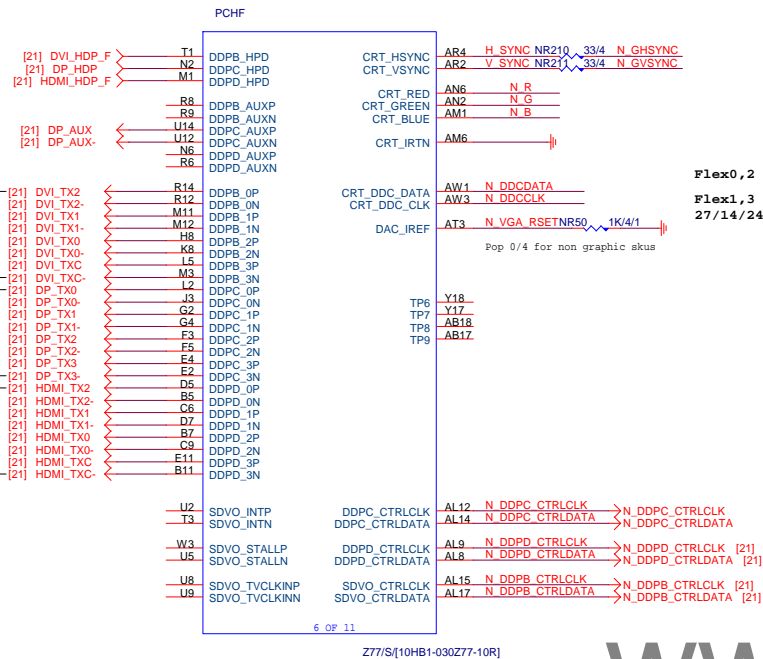
Z77/S[10HB1-030Z77-10R]



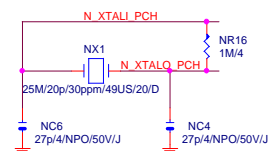
USB OC# Configure	
OC0#	F_USB30_1
OC1#	USB30_LAN1
OC2#	F_USB1
OC3#	F_USB2
OC4#	R_USB
OC5#	USB30_LAN2
OC6#	F_USB30_2_3
OC7#	Not Use

PCHE



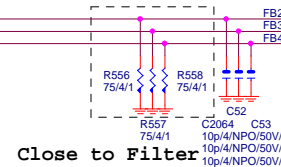
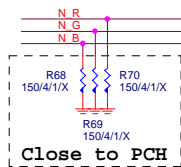
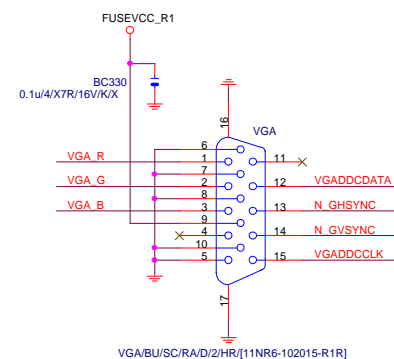
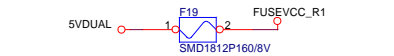
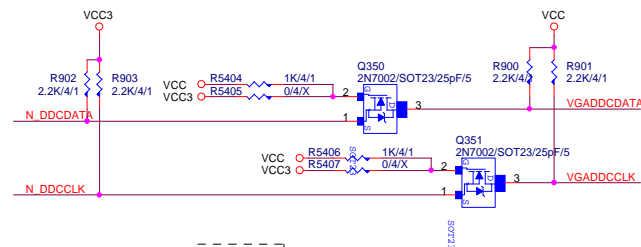
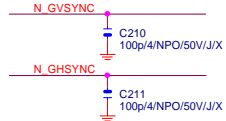
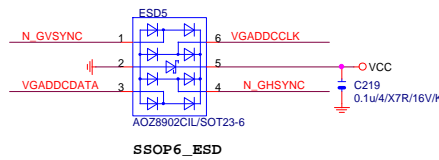
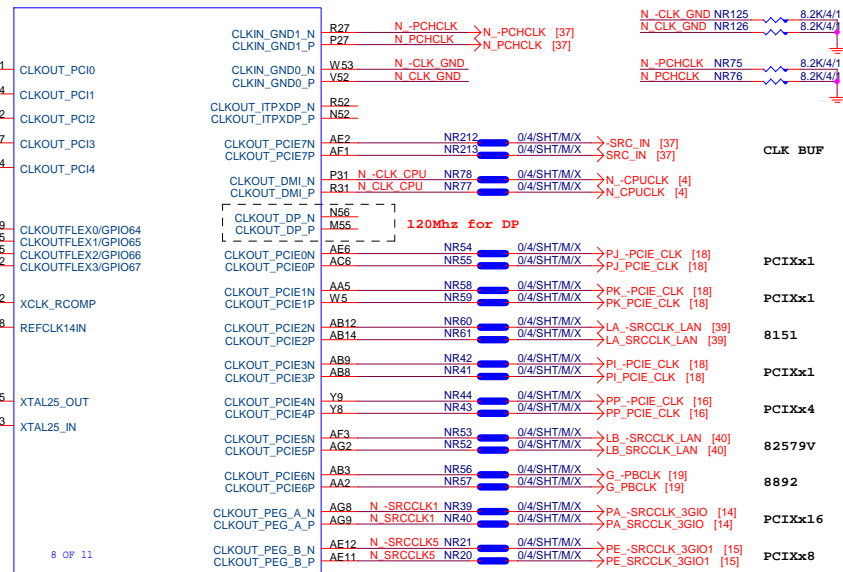


Flex0,2 : 33MHZ
 Flex1,3 : 27/14/24/48/25MHZ



N_PCHCLK14 NR33 8.2K/4/1

Mount for integrated clock Generation Mode



Gigabyte Technology			
Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number		Rev
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SATA:20/7.5/4.5/7.5/20 (breakout min 8/4/4/8)
Impedance=90 +- 17.5%

PCHC

PCHA

MB-ID

For WIFI

CL_CLK1

CL_DATA1

CL_RST1#

APWROK

PWM0

PWM1

PWM2

PWM3

TACH0/GPIO17

TACH1/GPIO1

TACH2/GPIO6

TACH3/GPIO7

TACH4_GPIO68

TACH5_GPIO69

TACH6_GPIO70

TACH7_GPIO71

SST

SCLOCK/GPIO22

SLOAD/GPIO38

SDATAOUT0/GPIO39

SDATAOUT1/GPIO48

CLKIN_SATA_N

CLKIN_SATA_P

SATALED#

SATAICOMP1

SATAICOMP0

SATA0GP/GPIO21

SATA1GP/GPIO19

SATA2GP/GPIO36

SATA3GP/GPIO37

SATA4GP/GPIO16

SATA5GP/GPIO49

AY20

NC_5

3 OF 11

NR177

0/4/SHT/MX

N ME PWROK

NC19

0.01u/4/X7R/25V/K/X

N GPIO17

N GPIO1

N GPIO6

N PHASE_CTRL

N GPIO68

N GPIO69

N GPIO70

N GPIO71

[34] N_SSTCTL

BC46

NC19

0.01u/4/X7R/25V/K/X

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N GPIO1

N GPIO6

N PHASE_CTRL

N GPIO68

N GPIO69

N GPIO70

N GPIO71

[34] N_SSTCTL

BC46

NC19

0.01u/4/X7R/25V/K/X

N GPIO17

N GPIO1

N GPIO6

N PHASE_CTRL

N GPIO68

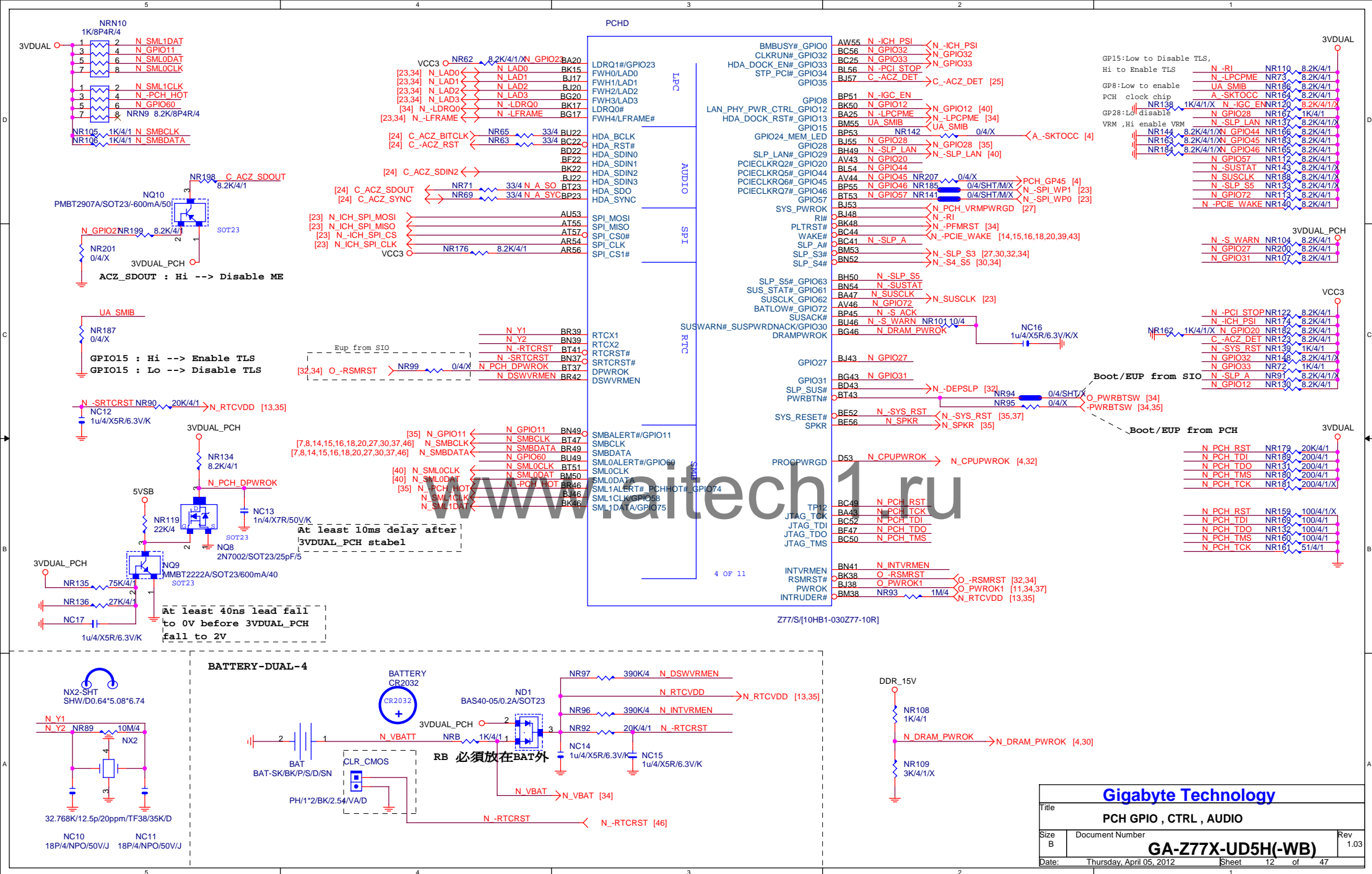
N GPIO69

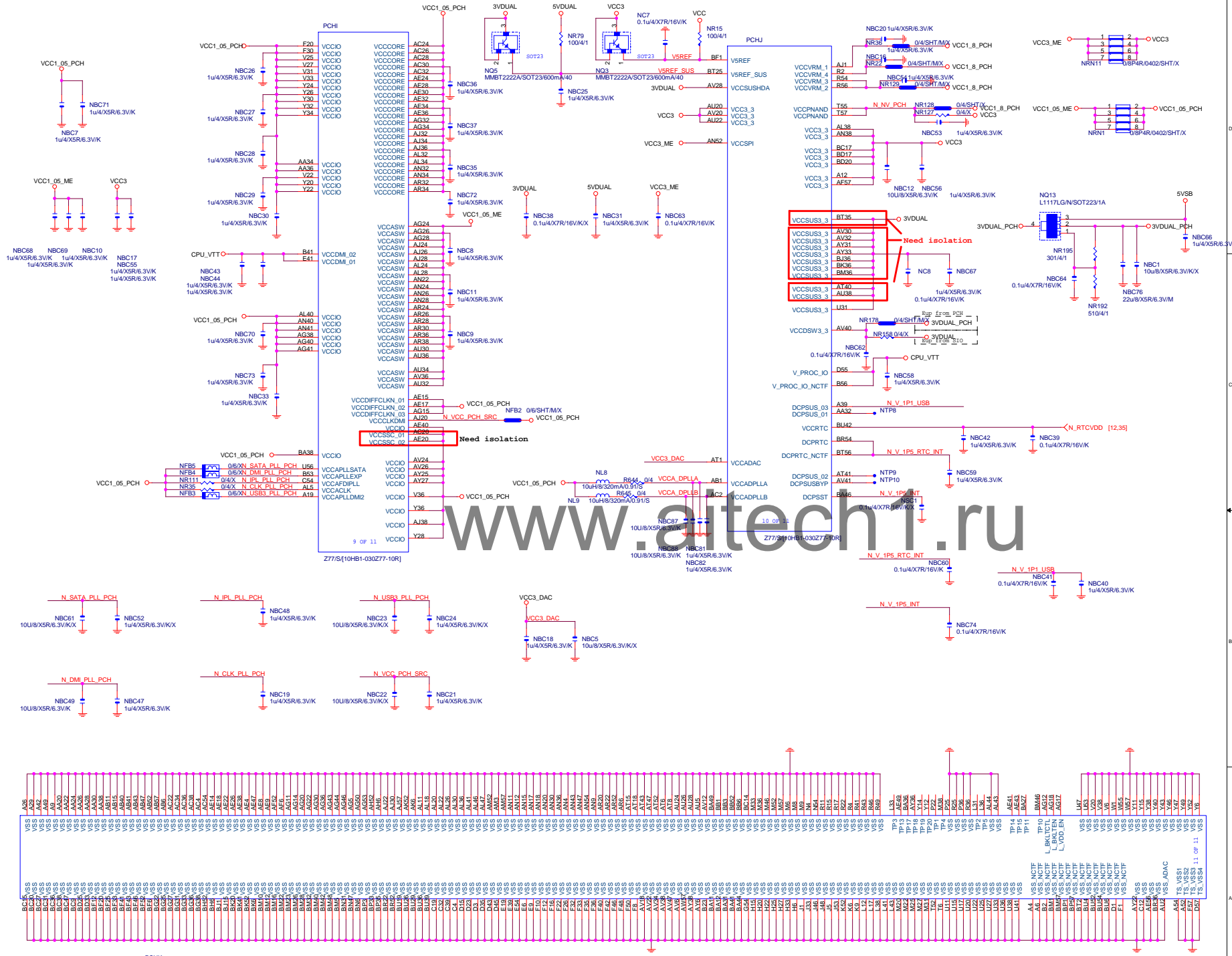
N GPIO70

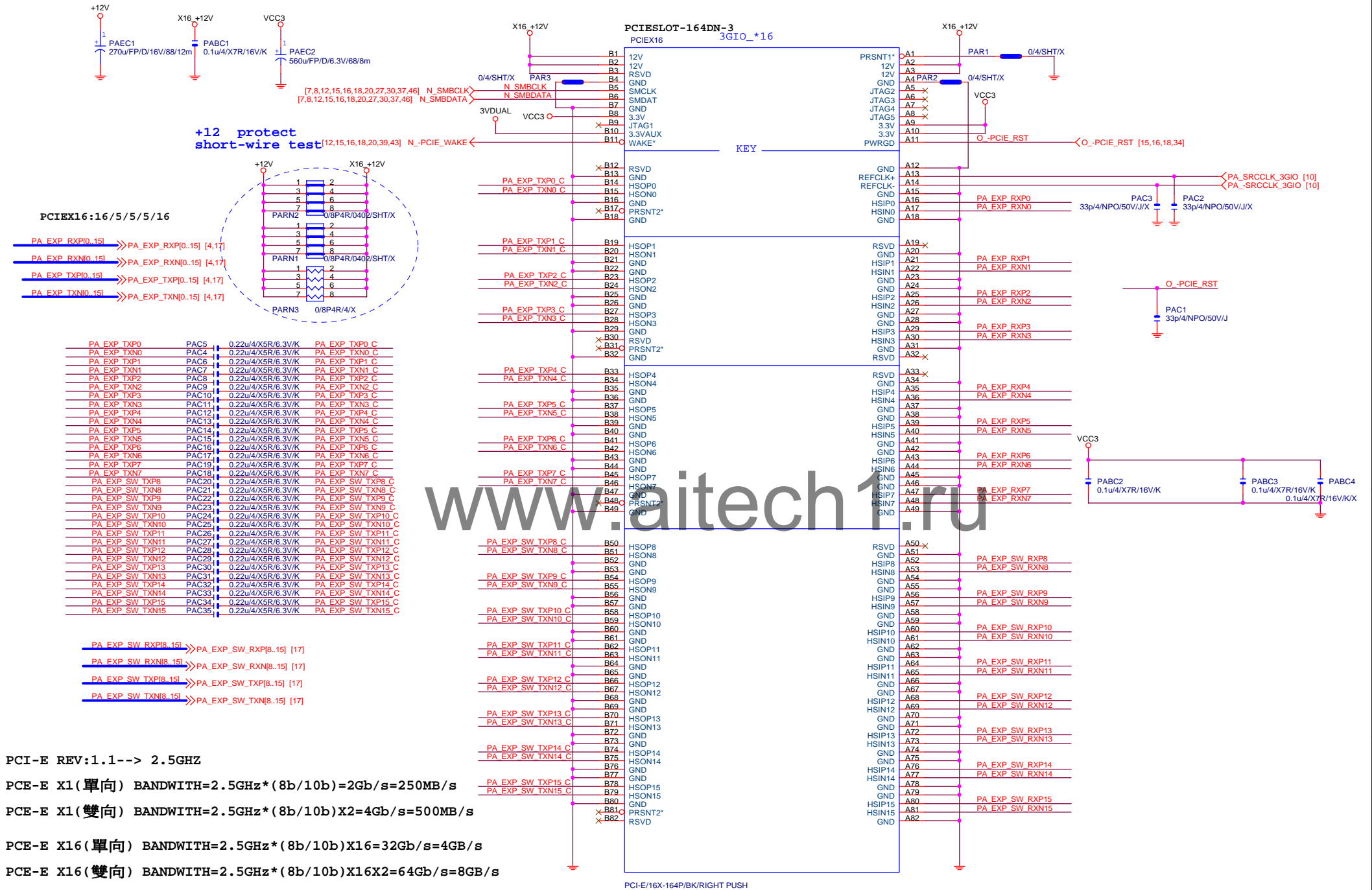
N GPIO71

[34] N_SSTCTL

BC46

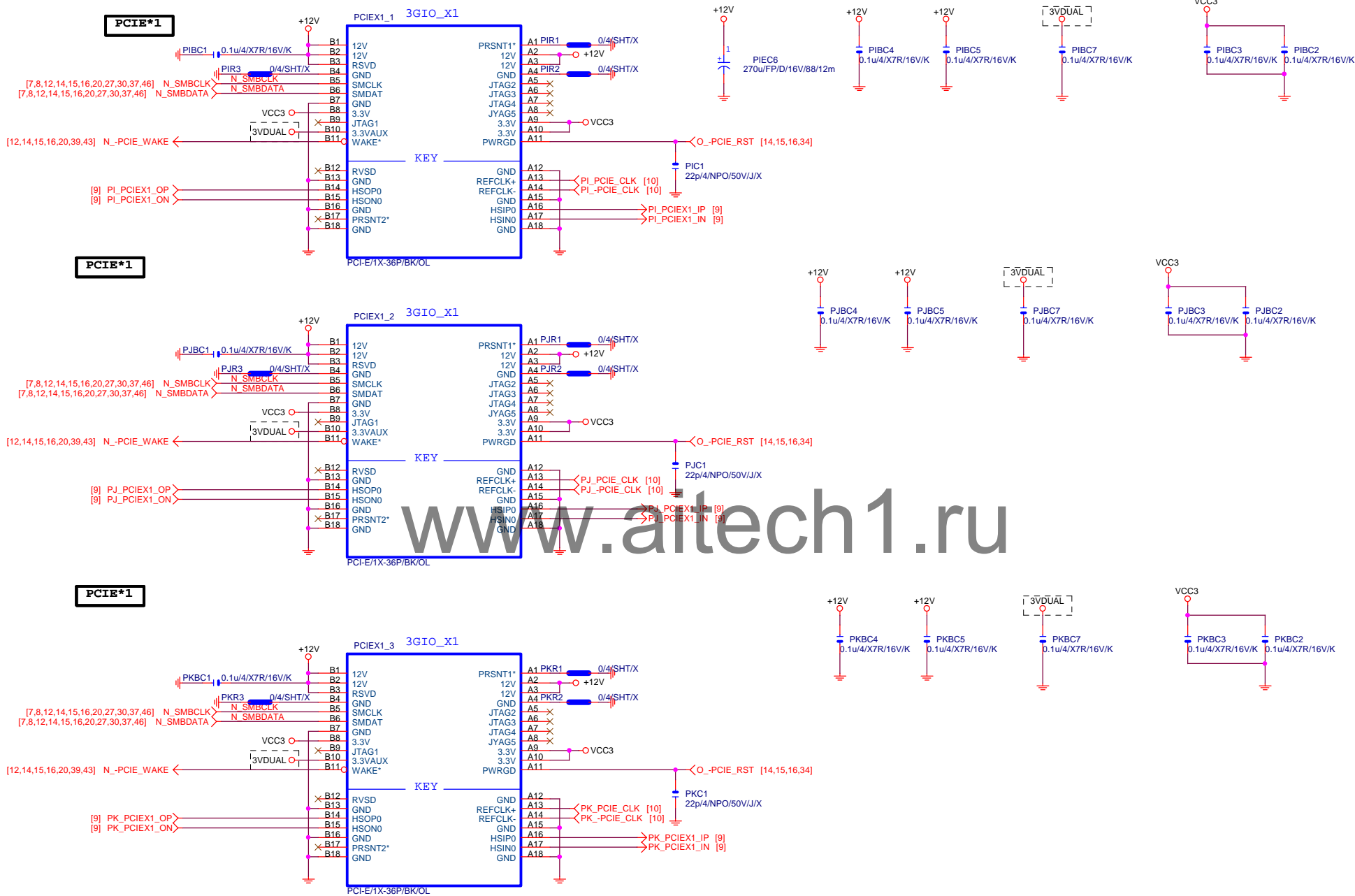


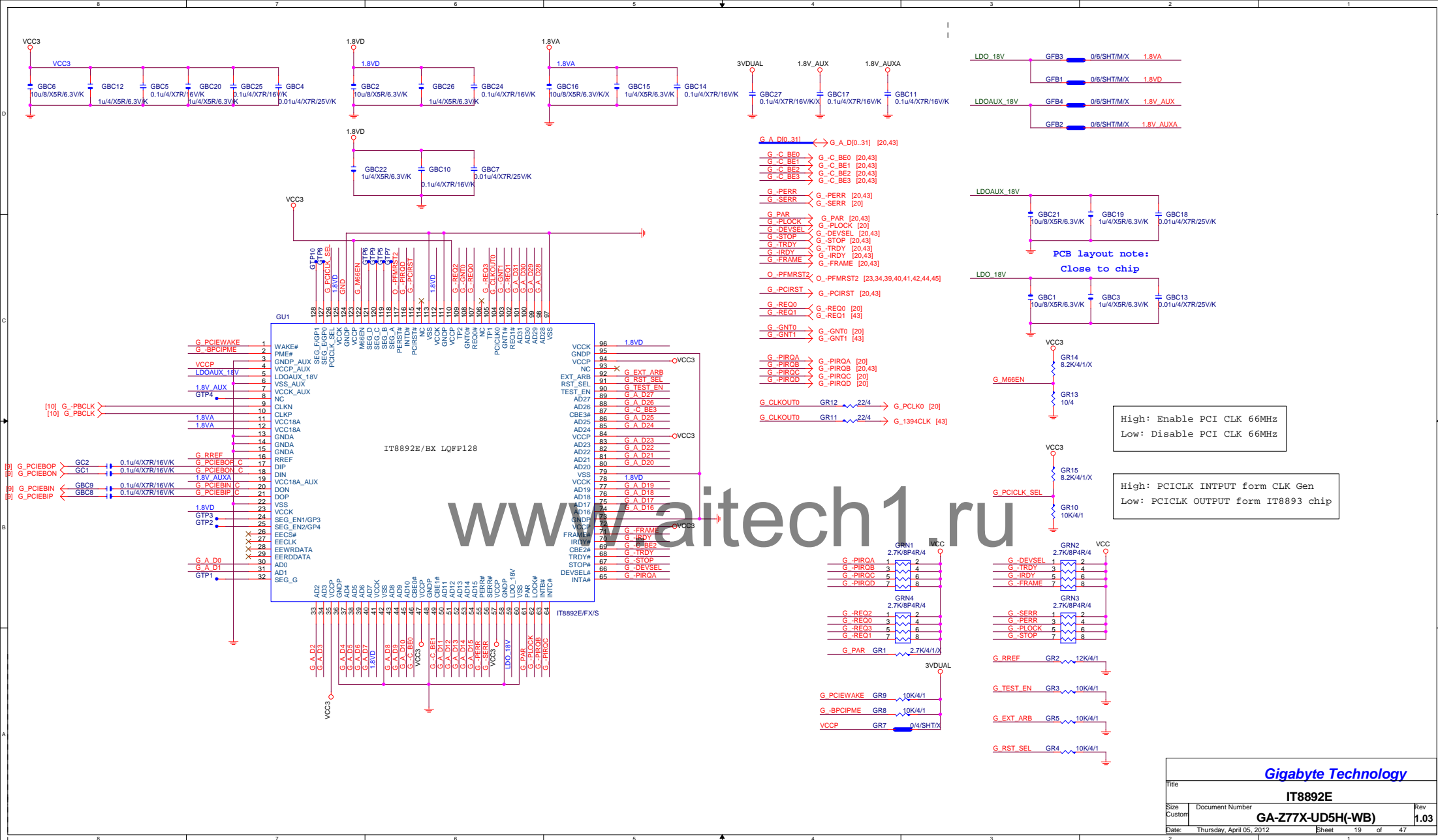




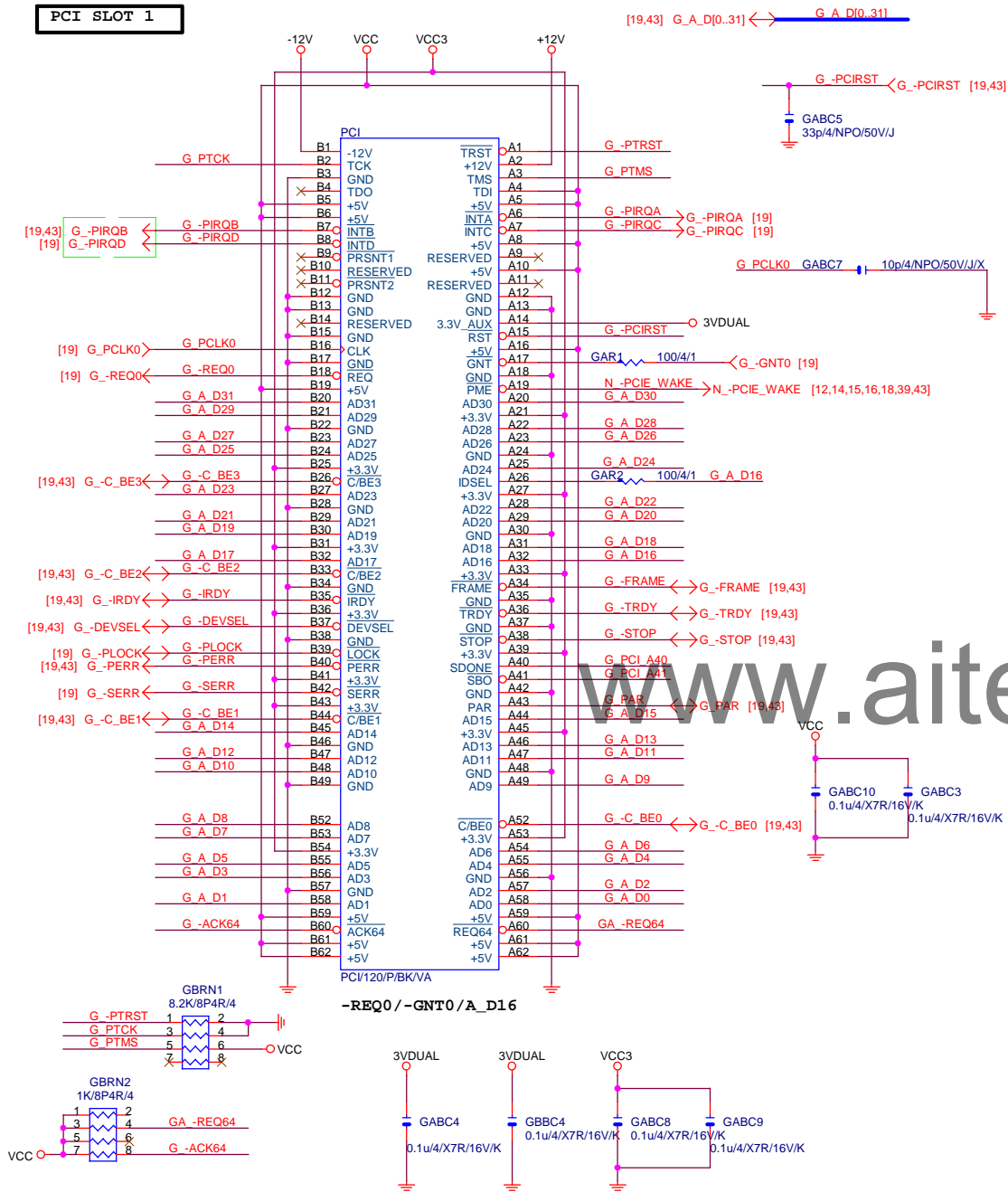
Gigabyte Technology

Title			
PCI EXPRESS * 16			
Size	Document Number	Rev	
Custom	GA-Z77X-UD5H(-WB)	1.03	
Date:	Thursday, April 05, 2012	Sheet	14 of 47



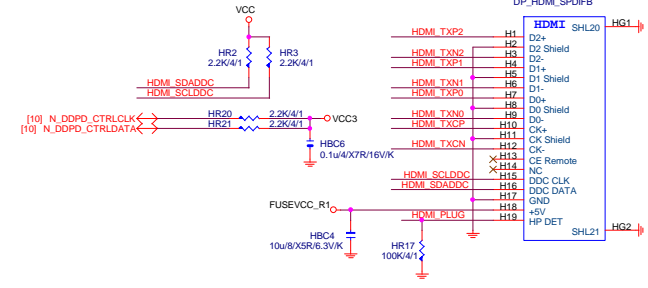


PCI SLOT 1

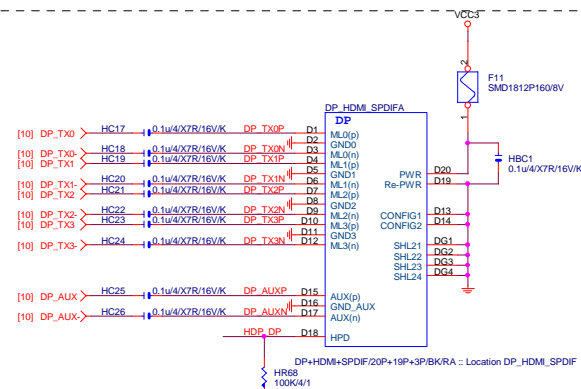
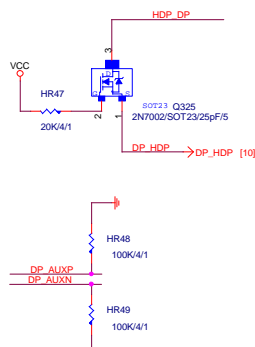
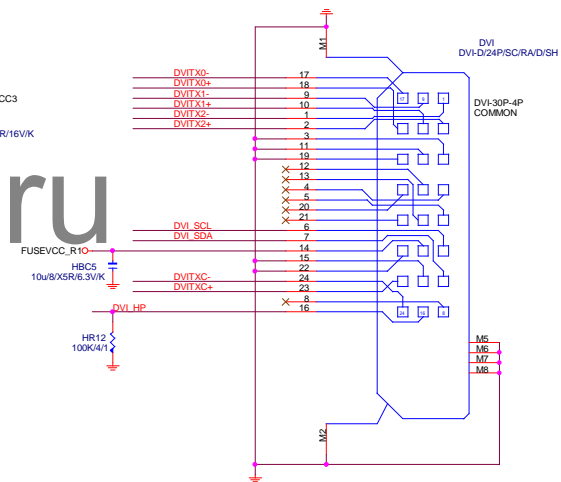
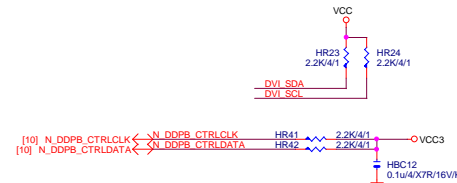


GIGABYTE™

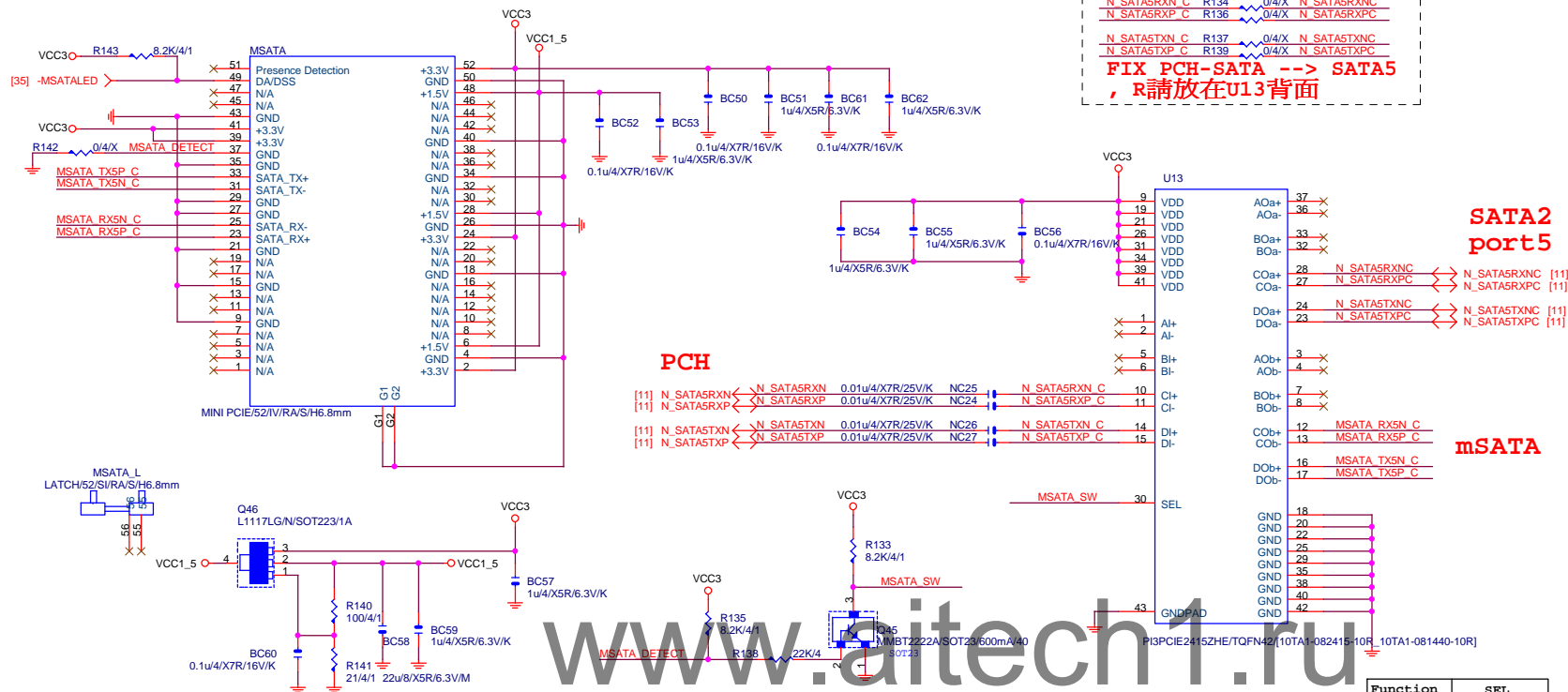
Title			PCI SLOT 1&2
Size	Document Number	Rev	
Custom		GA-Z77X-UD5H(-WB) 1.03	
Date:	Thursday, April 05, 2012	Sheet	20 of 47



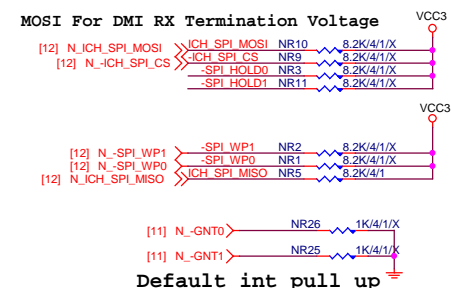
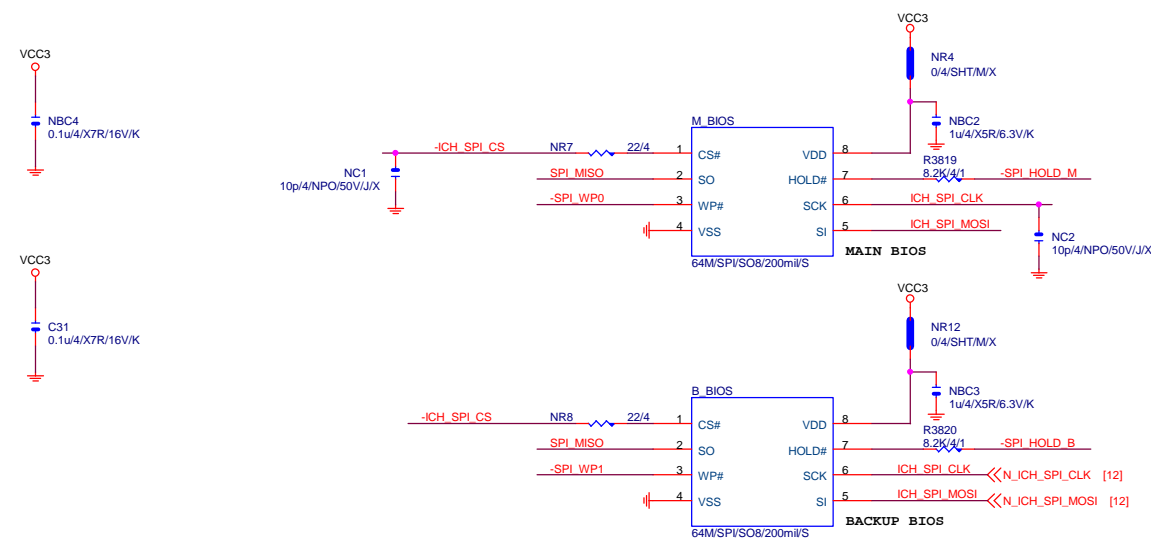
0 1:7.2dB



<i>Gigabyte Technology</i>			
Title HDMI / DVI/DP			
Size C	Document Number GA-Z77X-UD5H(-WB)		Rev 1.03
Date:	Thursday, April 05, 2012	Sheet 21 of 47	



Function	SEL
xI--> xOa	L
xI--> xOb	H

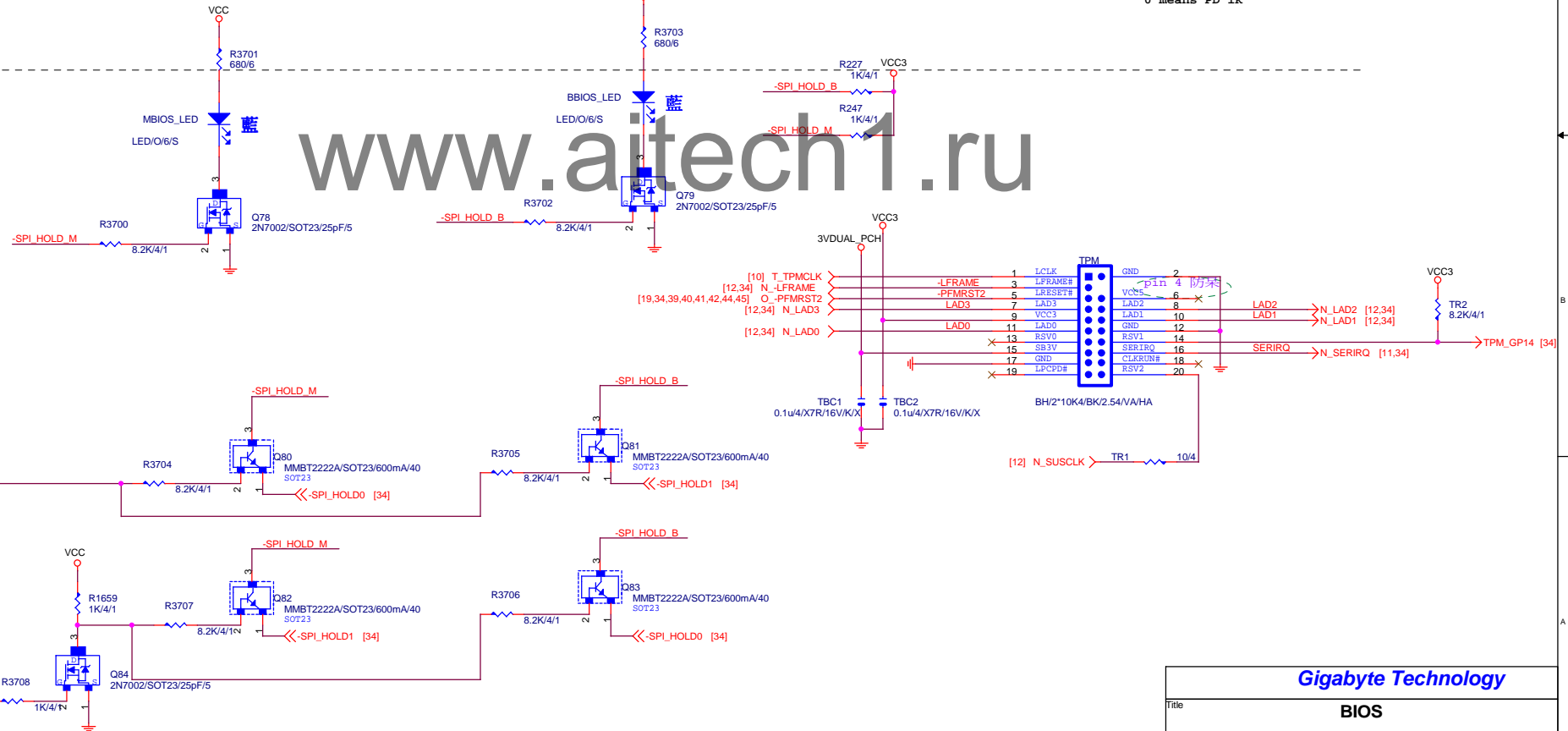


Default int pull up

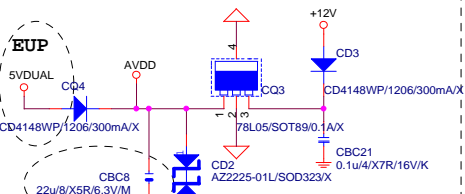


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

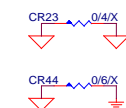
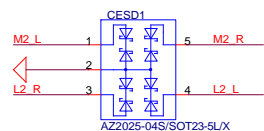
1 means floating
 0 means PD 1K



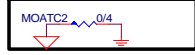
Gigabyte Technology	
Title HD AUDIO ALC889A	
Size Custom	Document Number GA-Z77X-UD5H(-WB)
Date: Thursday, April 05, 2012	Sheet 24 of 47



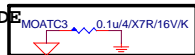
上ALC892時,此顆電容要保留



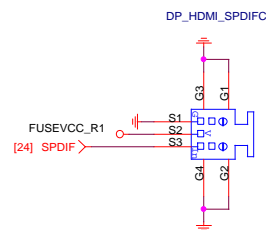
- Near Audio jack left



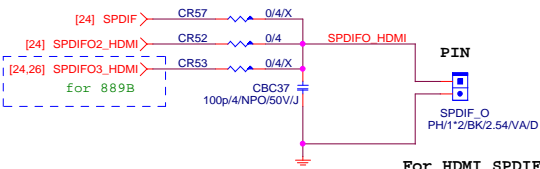
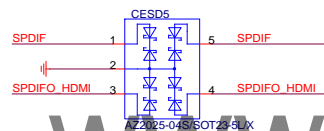
```
Codec --> Audio jack
```



F_AUDIO

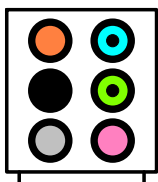


DP+HDMI+SPDIF/20P+19P+3P/BK/RA :: Location DP_HDMI_SPDIF

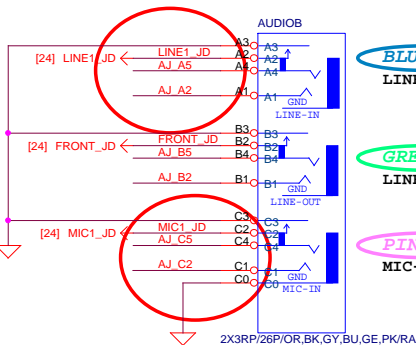
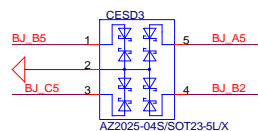
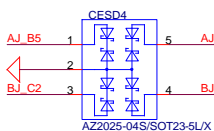
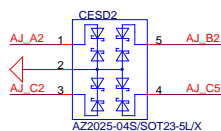


For HDMI SPDIF

BTX AZALIA CONNECTOR



11NR6-403007-21R

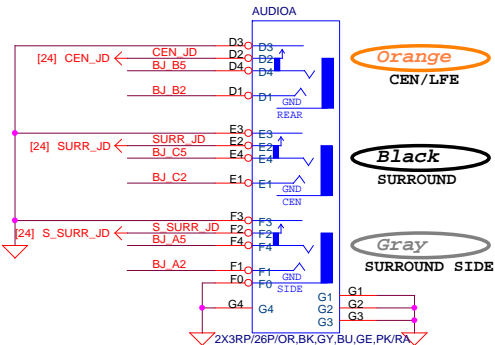


LINE-IN

GREEN

LINE-OUT

PINK



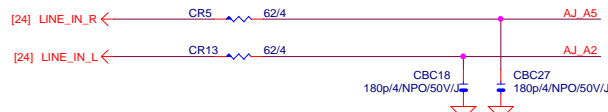
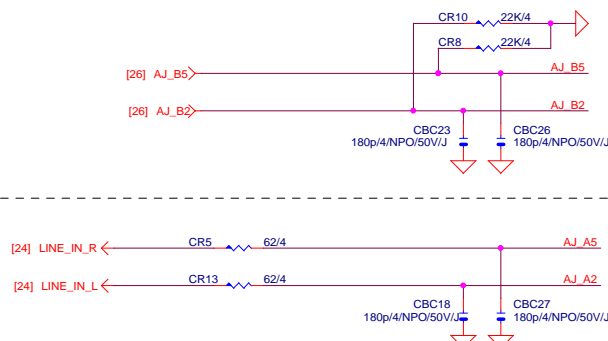
Orange

CEN/LFE

Black

SURROUND

Gray

[illegible]

EMI

CEC5 100uS/D/16V/66/30m

CEC7 100uS/D/16V/66/30m

CR46 62K/4

CR19 62K/4

CR20 22K/4

CR45 22K/4

[24] SURR_R

[24] SURR_L

BJ C5

BJ C2

[illegible]

AZALIA FRONT PANEL

Diagram showing the front panel components and connections for the AZALIA system. The diagram is divided into a **Digital Area** (indicated by a red diagonal line) and an **EMI** (Electromagnetic Interference) section.

Components and Connections:

- Power and Biasing:**
 - BAT54A/SOT23/200mA (Diode)
 - CQ2 (Capacitor)
 - CR25 (8.2K/4/1/X)
 - CR15 (8.2K/4/1/X)
 - CR12 (8.2K/4/1)
 - CR3 (8.2K/4/1)
- Microphone Inputs:**
 - MIC2_VREF0 (24-pin connector)
 - MIC2_L (24-pin connector)
 - MIC2_R (24-pin connector)
 - L2_L (26-pin connector)
 - L2_R (26-pin connector)
- Audio and Other Inputs:**
 - AUDIO_ID (26-pin connector)
 - M2_L (52/4)
 - M2_R (52/4)
 - CBC10 (180p/4/NPO/50V/J)
 - CBC16 (180p/4/NPO/50V/J)
 - CBC17 (180p/4/NPO/50V/J)
 - CBC6 (180p/4/NPO/50V/J)
- Output and Control:**
 - 3VDUAL (3V DUAL)
 - C-ACZ_DET [12] (12-pin connector)
- Other Components:**
 - CR27 (22K/4)
 - CR26 (22K/4)
 - CR35 (20K/4/1)
 - CR31 (39.2K/4/1)
 - CR56 (8.2K/4/1/X)

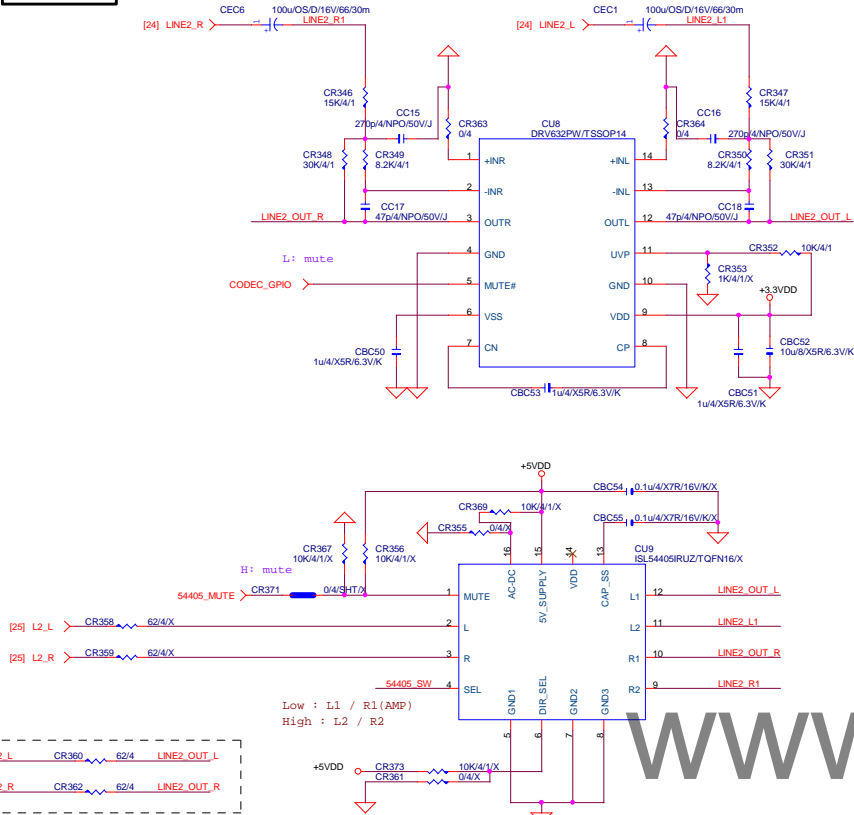
The diagram also includes a **Digital Area** section, which is separated from the rest of the circuit by a red diagonal line. This area contains components like CR27, CR26, CR35, CR31, and CR56, which are connected to the 3VDUAL and C-ACZ_DET [12] connectors.

A Digital Area

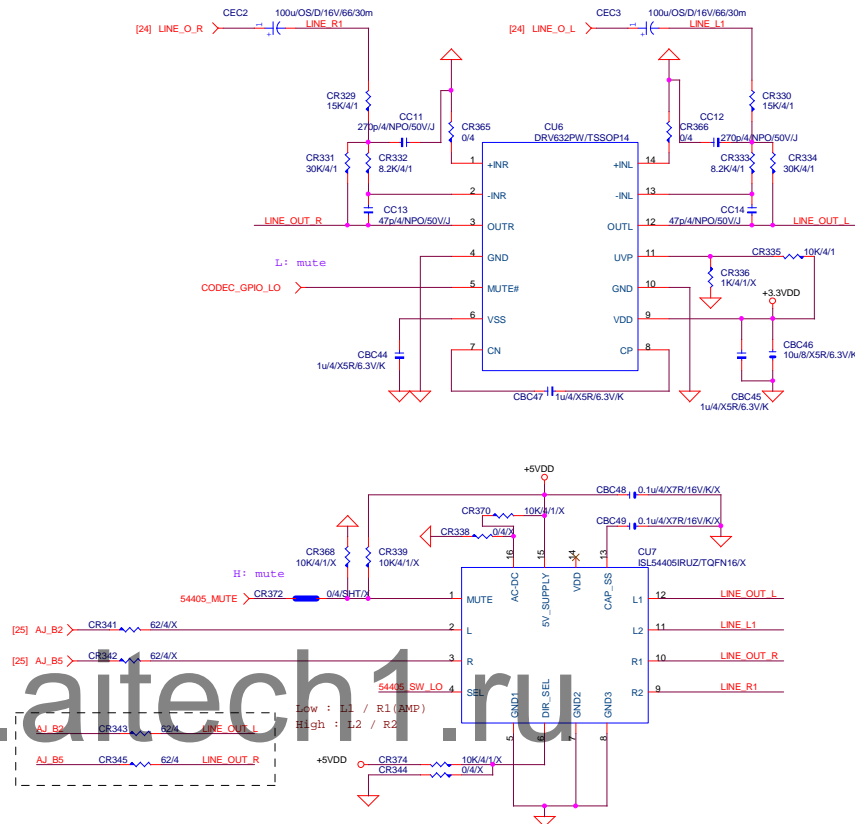
Gigabyte Technology

Title					AUDIO JACK				
Size Custom		Document Number		GA-Z77X-UD5H(-WB)					Rev 1.03
Date: Thursday, April 05, 2012				Sheet		25		of 47	

HEADPHONE



LINE-OUT



HEADPHONE

AMP_CODEC for 889
AMP_CODEC1 for 898/887-VD2
[24,25] AMP_CODEC ← CR256 10K/4/X
[24] AMP_CODEC1 ← CR320 10K/4/X
LOW : NORMAL
HIGH : AMPLIFY
inbox driver default low
Realtek driver 為 high

LINE-OUT

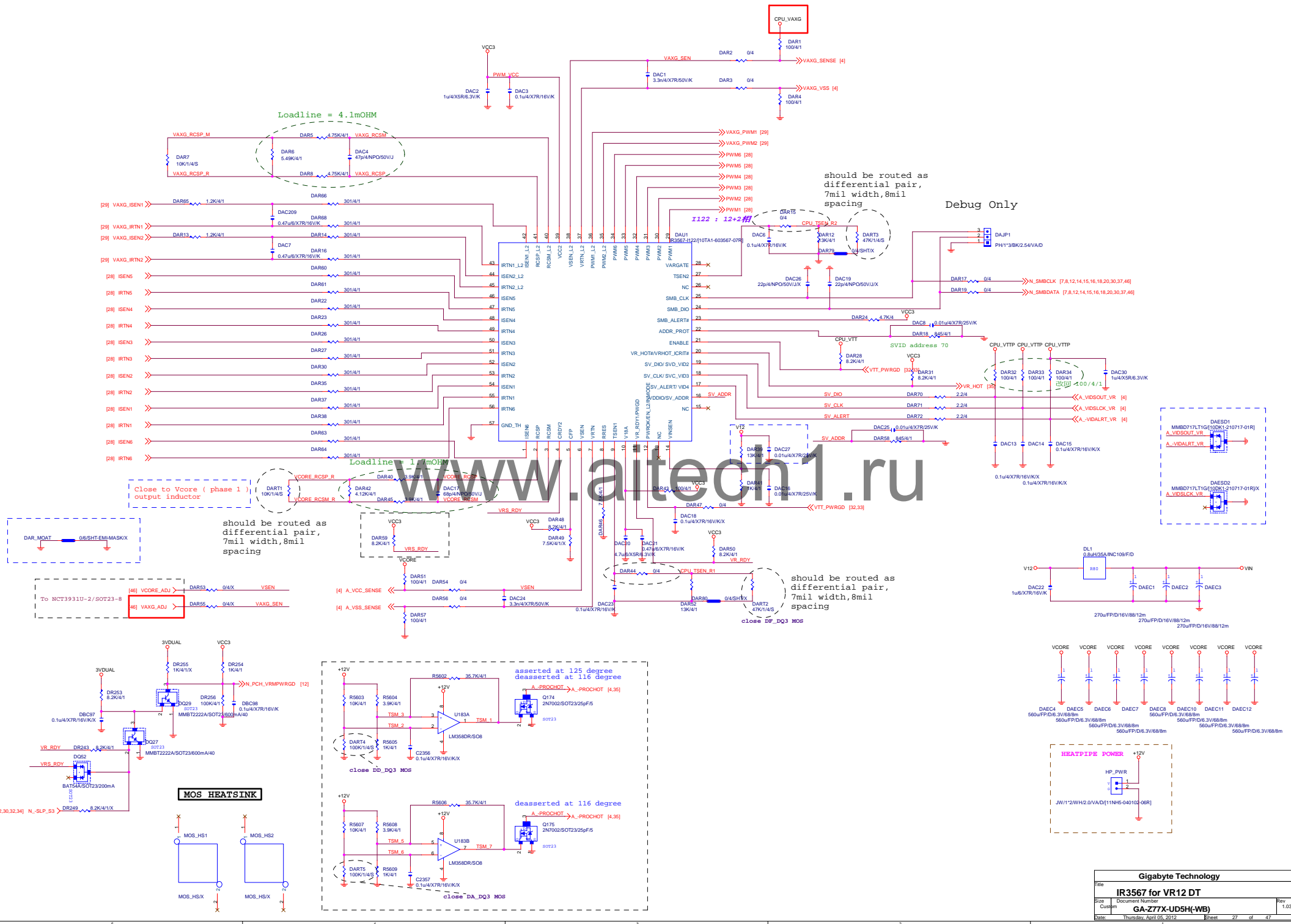
LOW : NORMAL
HIGH : AMPLIFY
inbox driver default low
Realtek driver 為 high

[24] -EAPD
default low, 進作業系統
(inbox/Realtek driver)為high

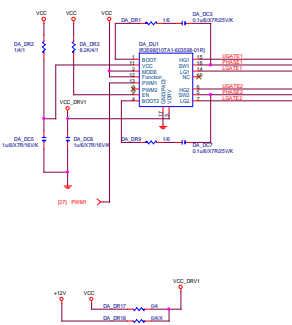
CODEC_GPIO CR354 0/4/X CODEC_GPIO_LO
54405_SW CR382 0/4/X 54405_SW_LO

Gigabyte Technology

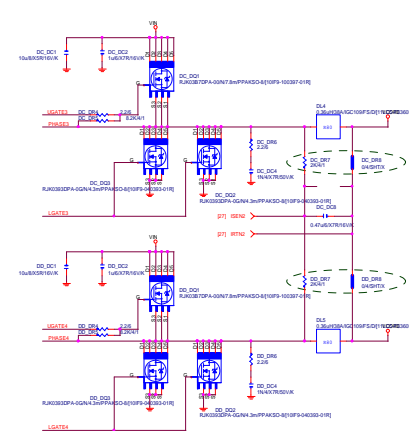
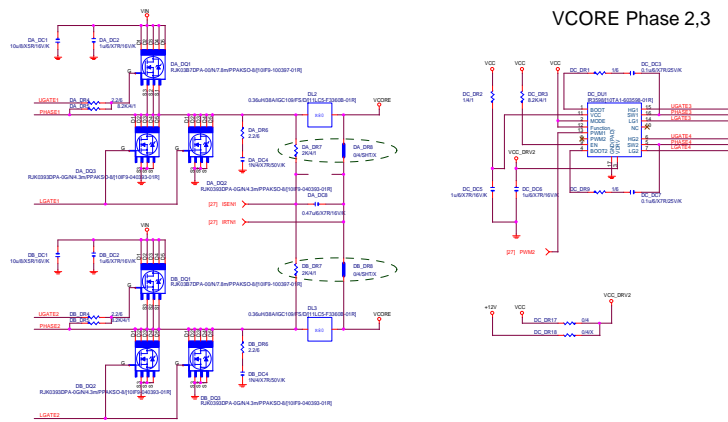
Title		8-CH DAC & Anti-Pop / Mute	
Size	Document Number	GA-Z77X-UD5H(-WB)	
Custom		1.03	
Date:	Thursday, April 05, 2012	Sheet	26 of 47



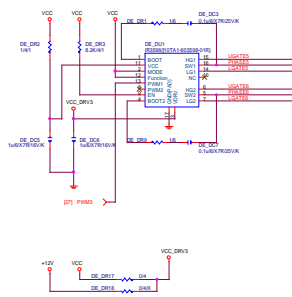
VCORE Phase 1,2



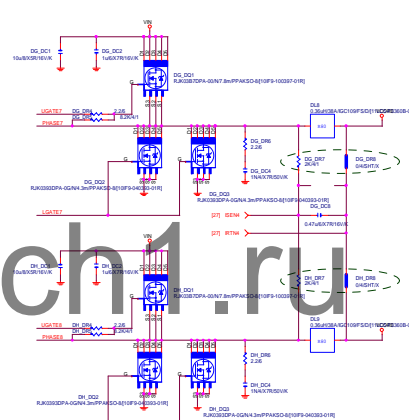
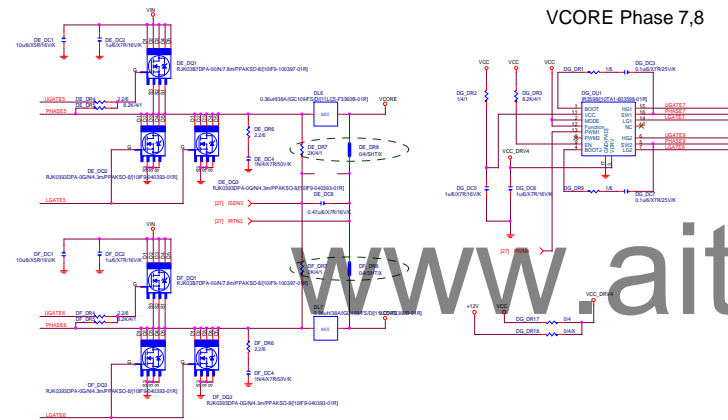
VCORE Phase 2,3



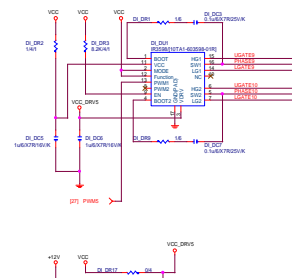
VCORE Phase 5,6



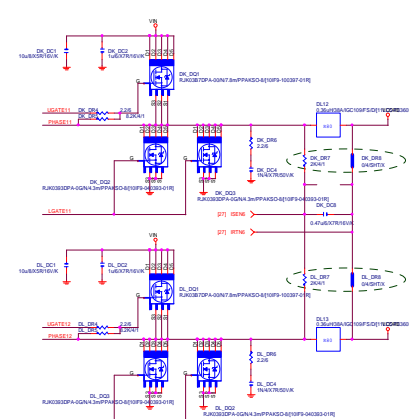
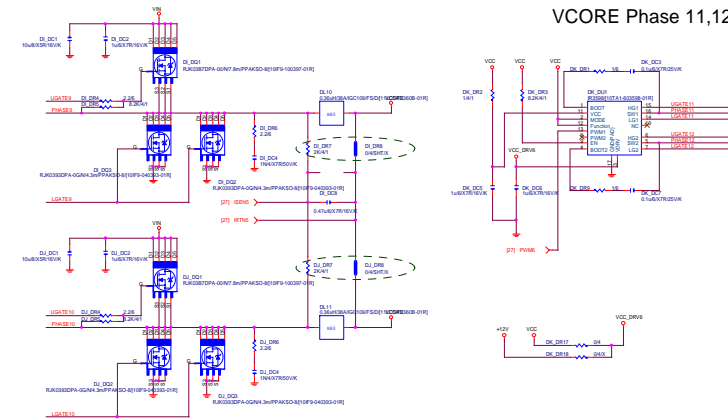
VCORE Phase 7,8

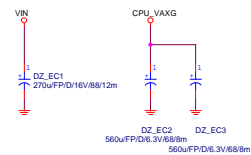
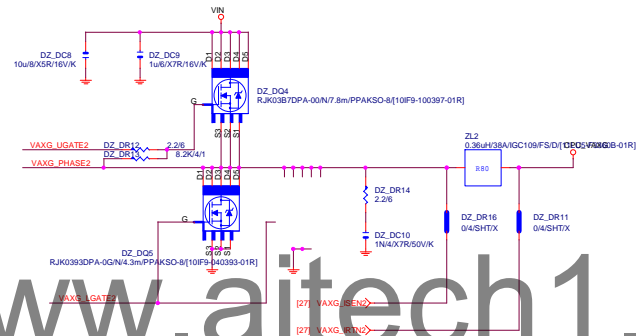
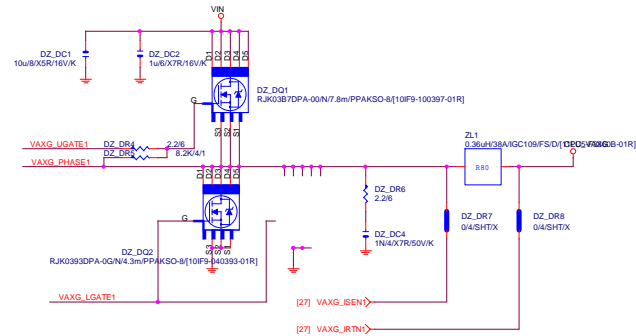


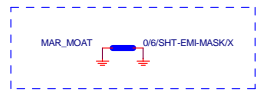
VCORE Phase 9,10



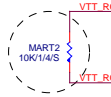
VCORE Phase 11,12



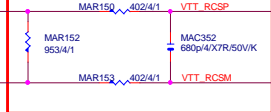
[illegible]



Close to VTT output inductor



Value need check with Vendor



[31] VTT_ISEN1

[31] VTT_IRTN1

[31] MA_ISEN2

[31] MA_IRTN2

[31] MA_ISEN1

[31] MA_IRTN1

Value need check with Vendor



Close to DDR output inductor

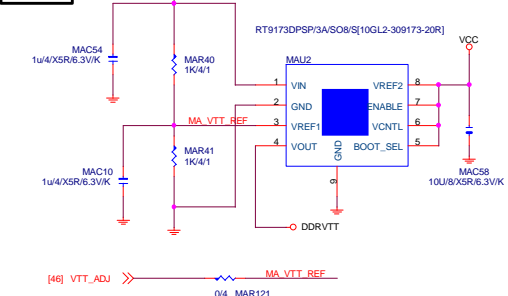


should be routed as differential pair, 7mil width, 8mil spacing

[46] DDR15V_ADJ1

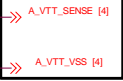
For power sequence, VTT enable VSA, then VSA enable Vcore

DDRVTT



For power sequence require

[46] VTTD_ADJ1



To CPU pin AB3,AB4

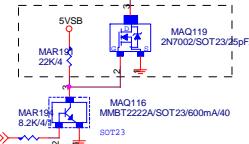
IR3570

Addr: 72h

www.aitech1.ru

Link to PCH pin BQ46

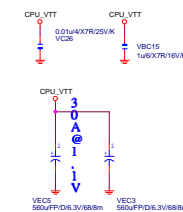
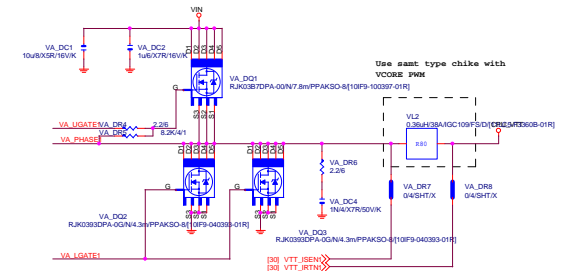
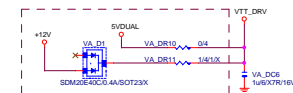
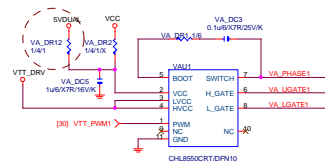
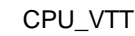
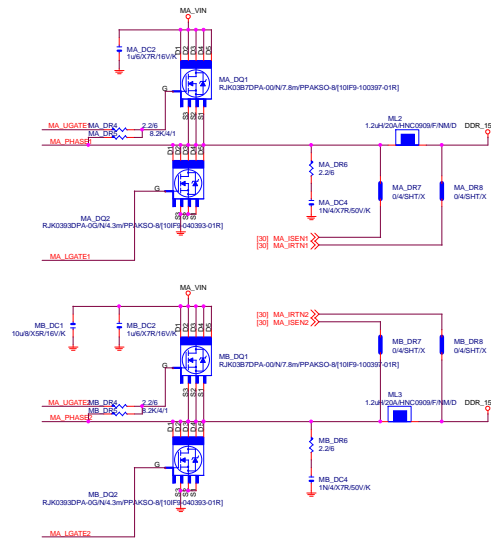
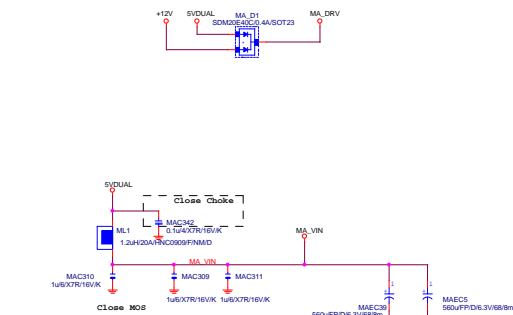
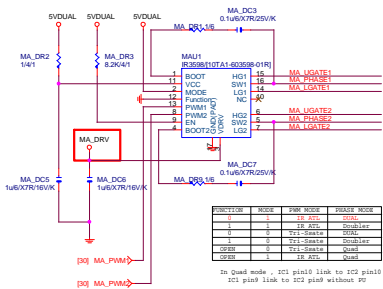
Full up in PCH side

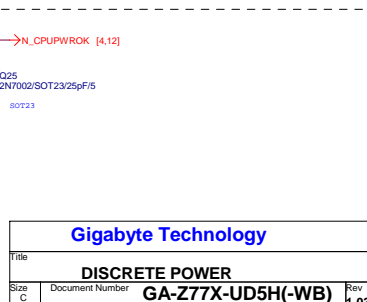
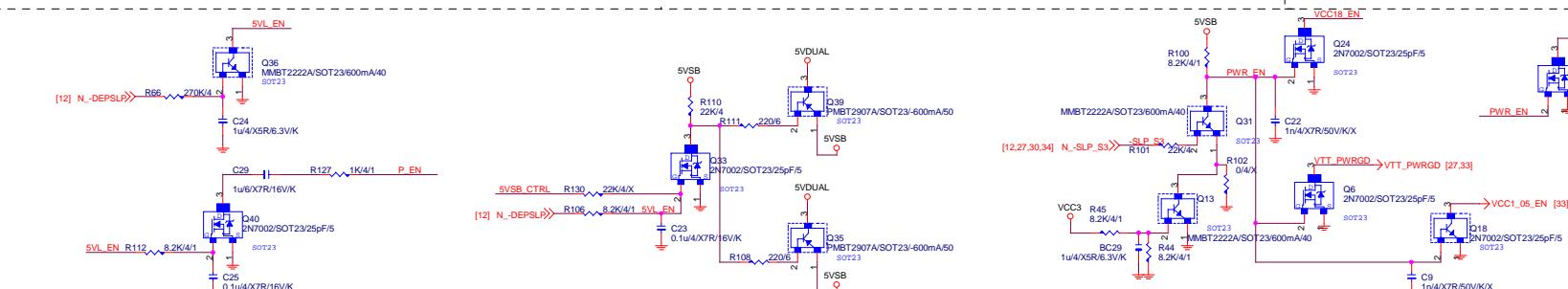
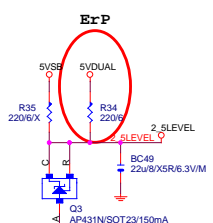
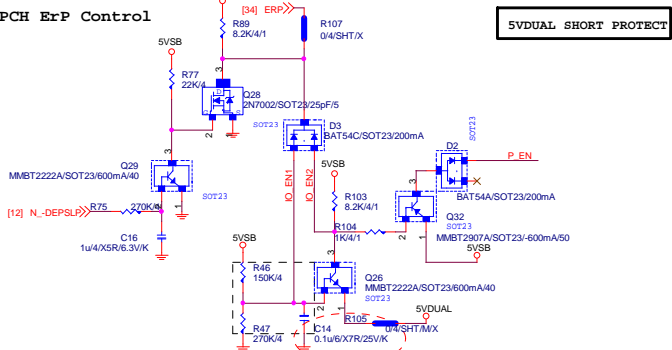
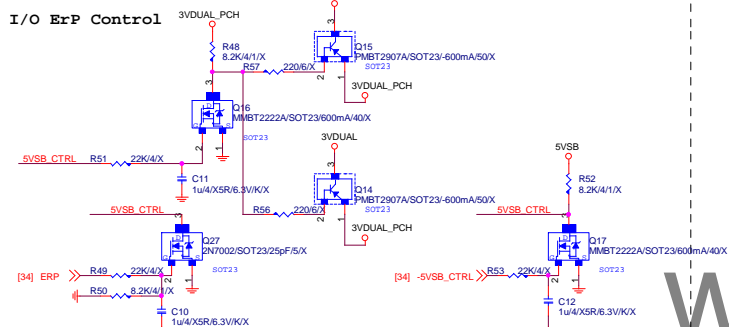
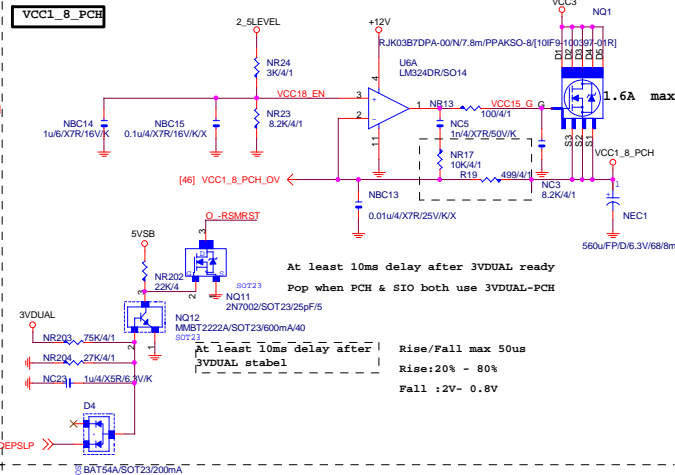
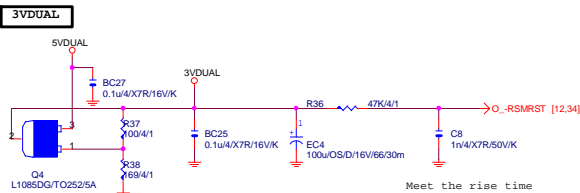
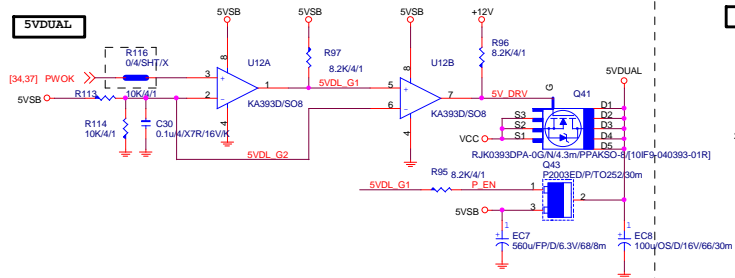


[12.34] N_S4_Ss

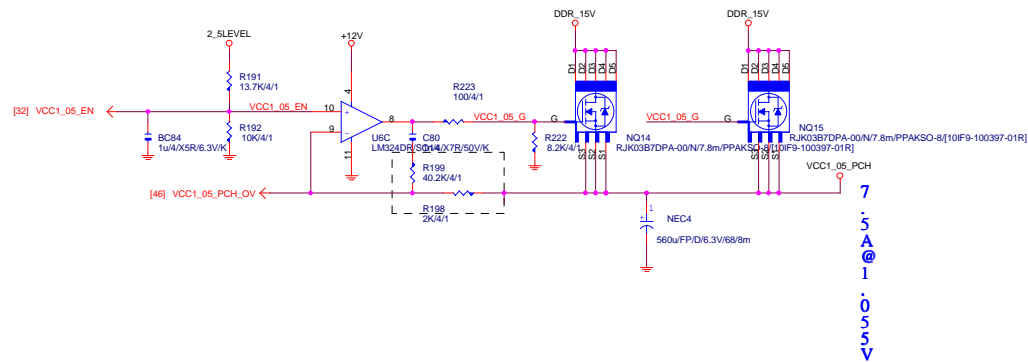
GIGABYTE			
Title			
DDR & CPU_VTT POWER IR3570			
Size	Document Number	Rev	
C	GA-Z77X-UD5H(-WB)	1.03	
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DDR_15V



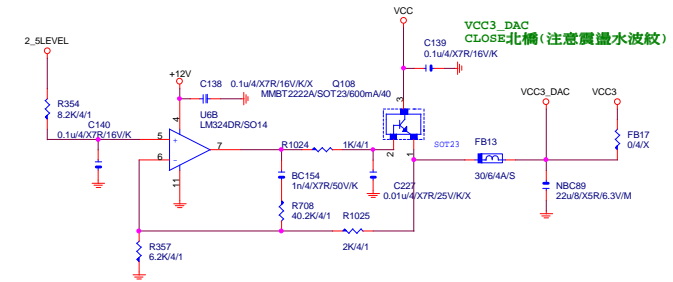


VCC1_05_PCH

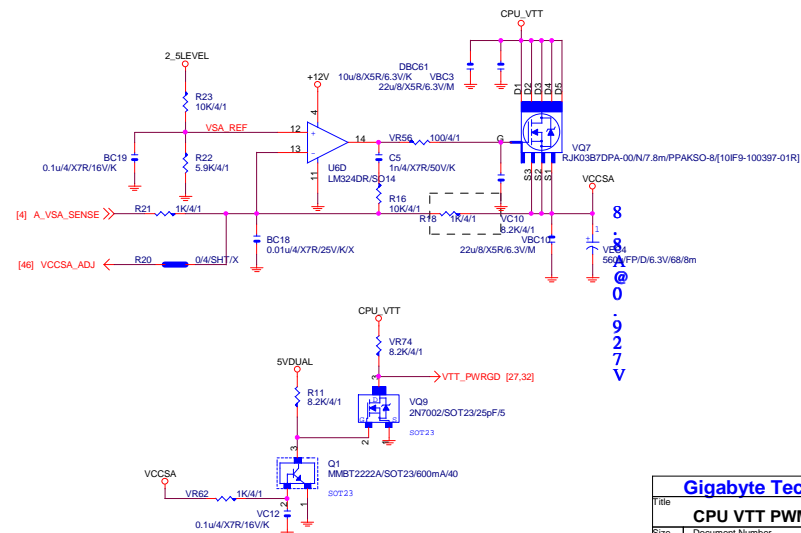
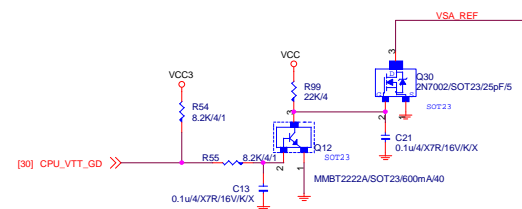


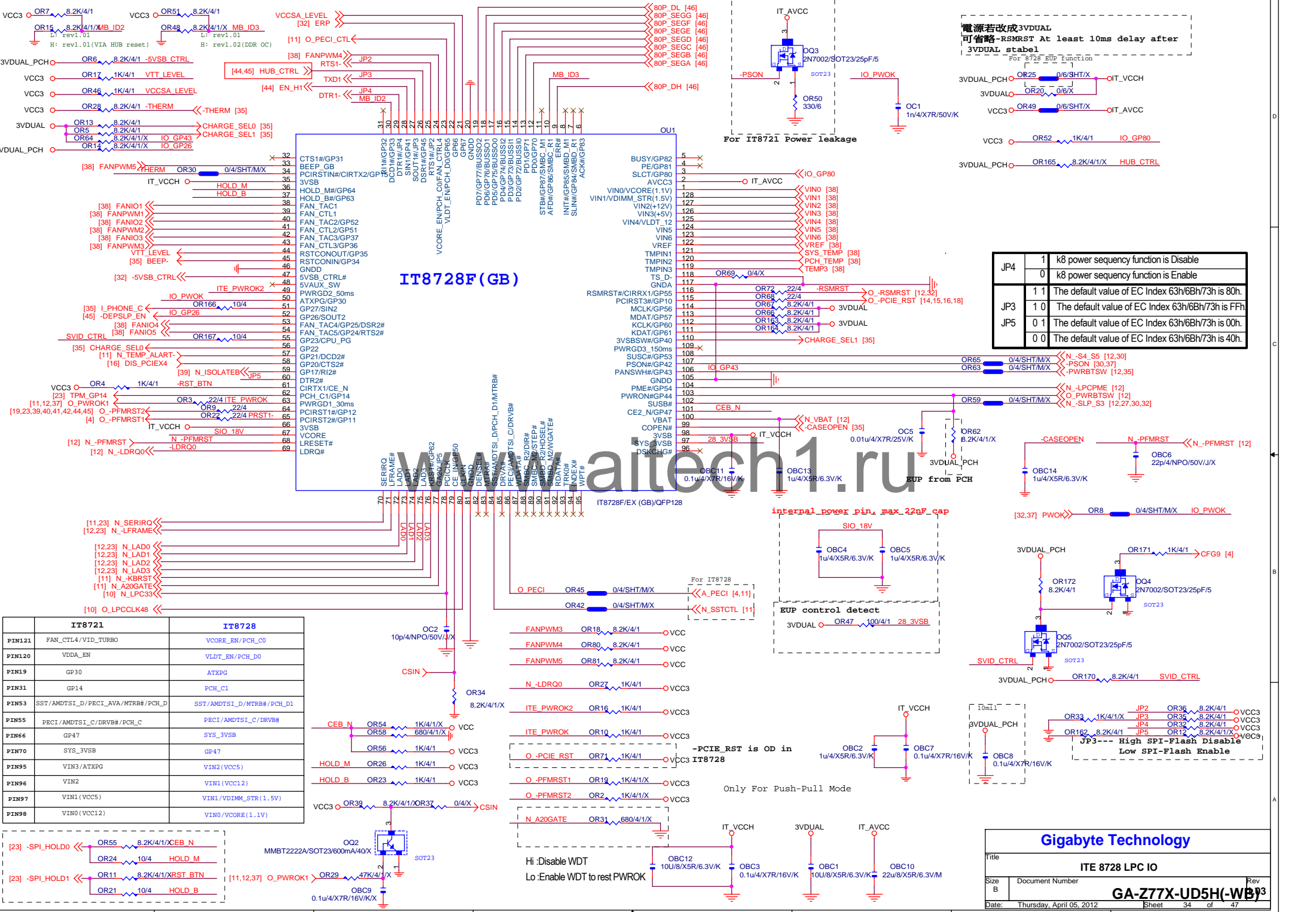
VCC3_DAC

(3.3V/70mA+360uA)



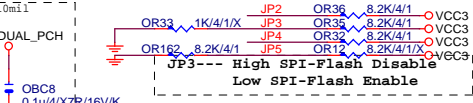
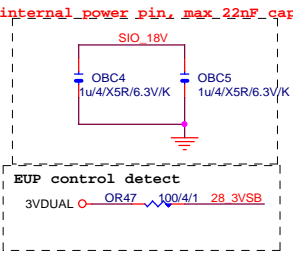
VCC_SA

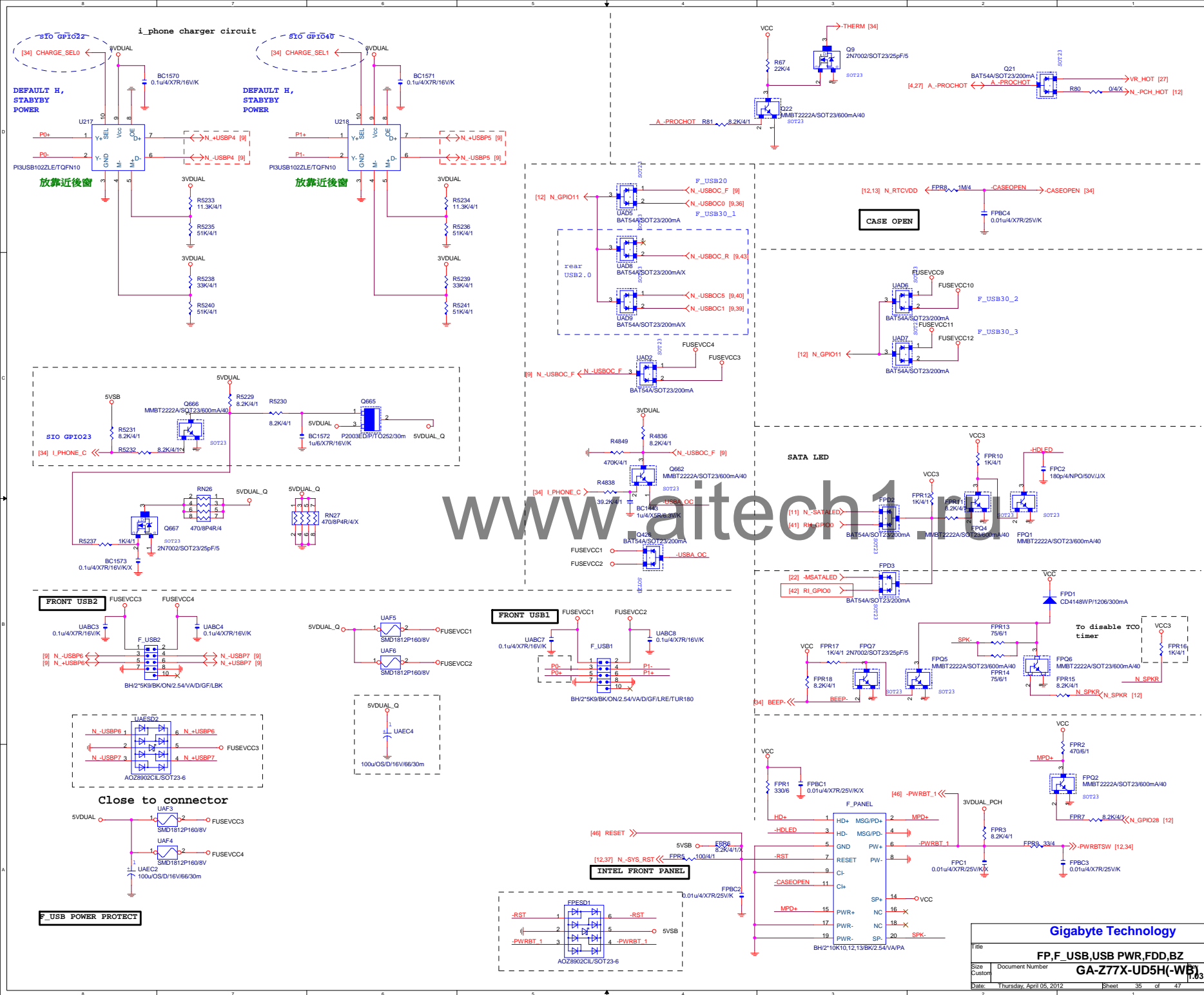


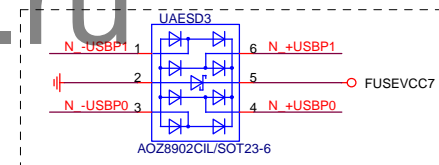
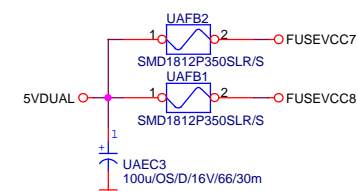
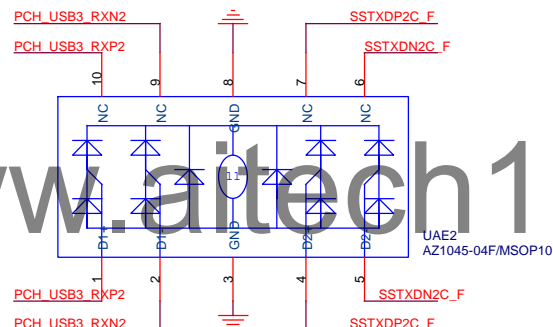
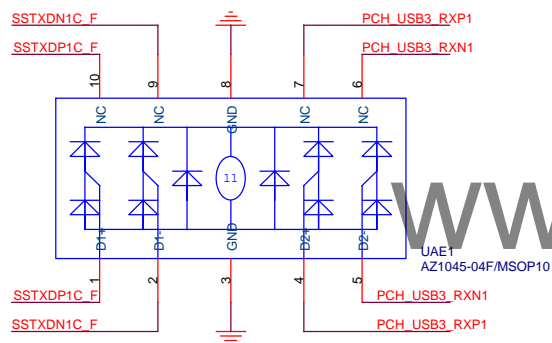
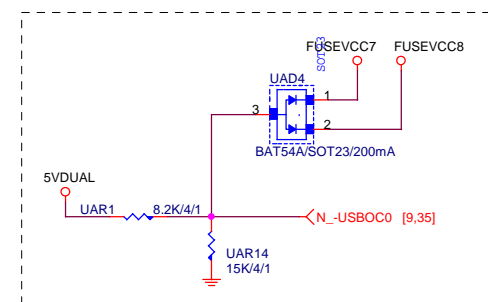
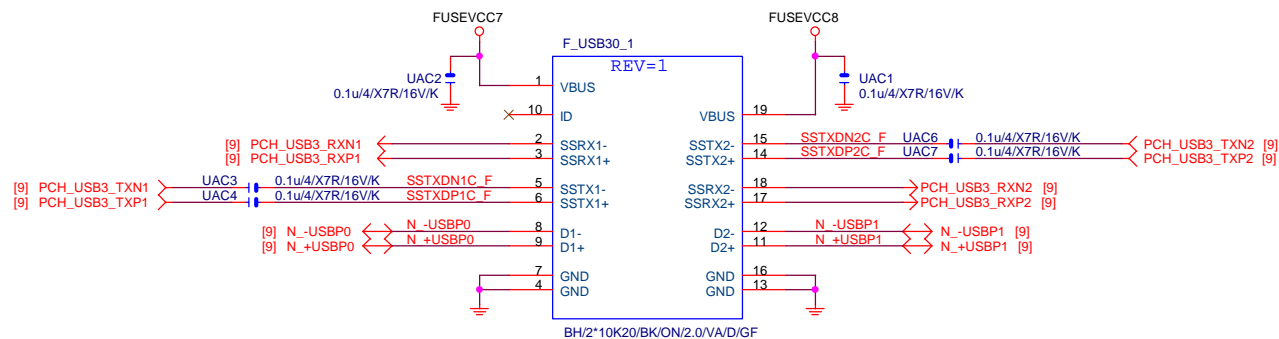


電源若改成3VDUAL
可省略-RSMRST At least 10ms delay after
3VDUAL stabl
For 8728 EUP Function

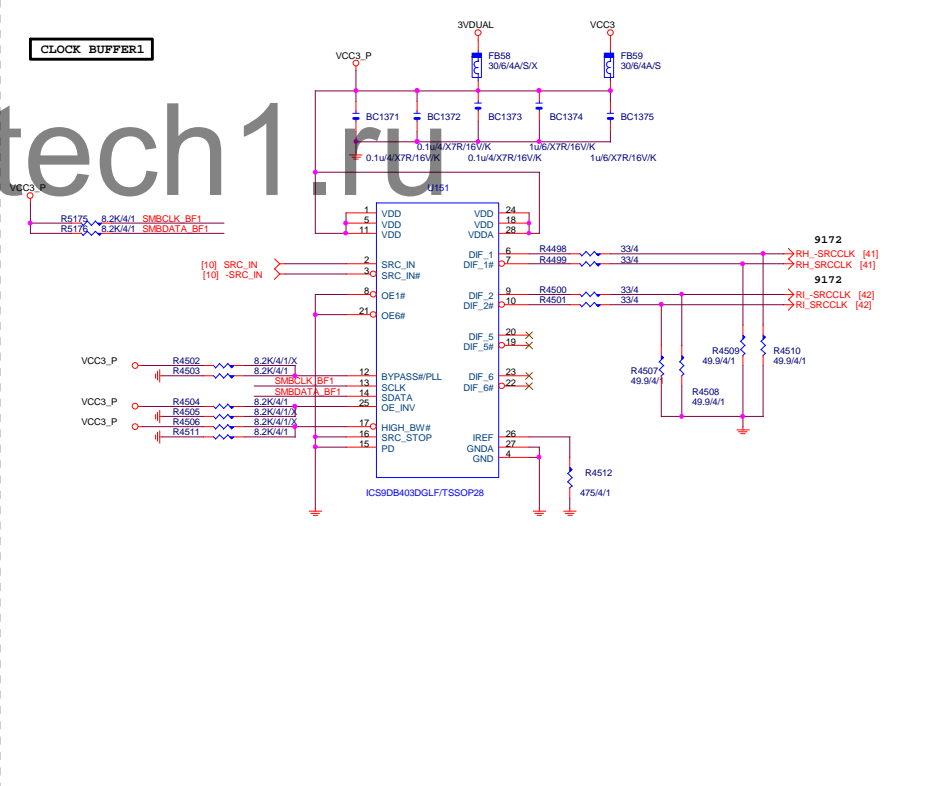
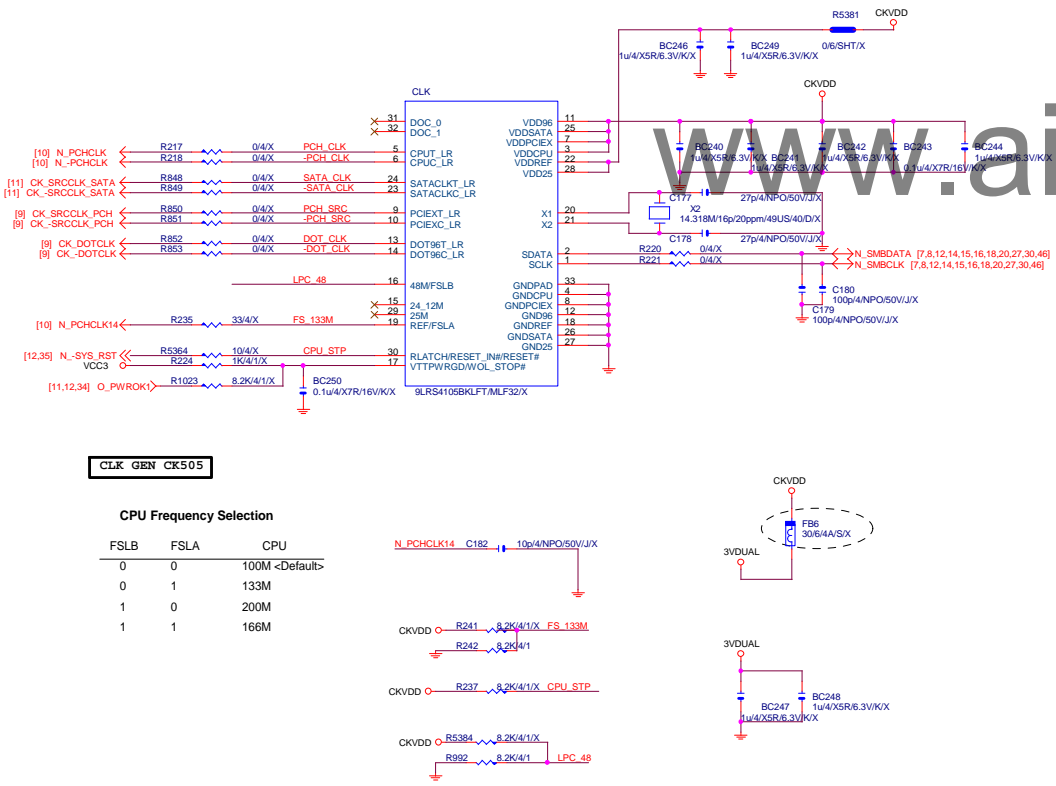
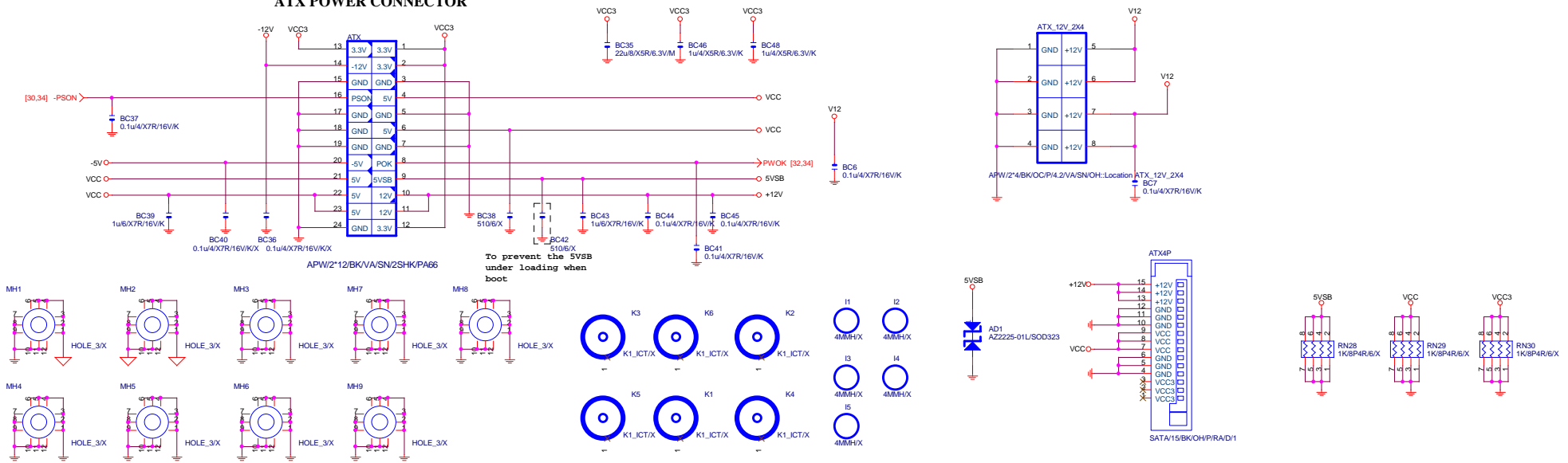
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.



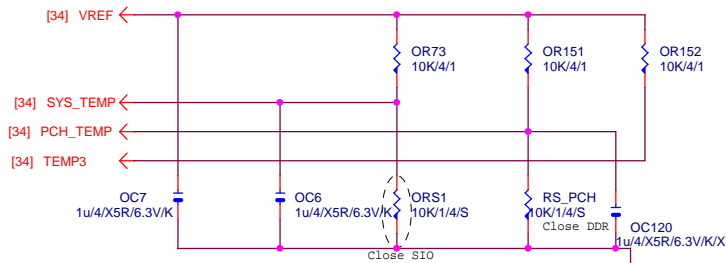




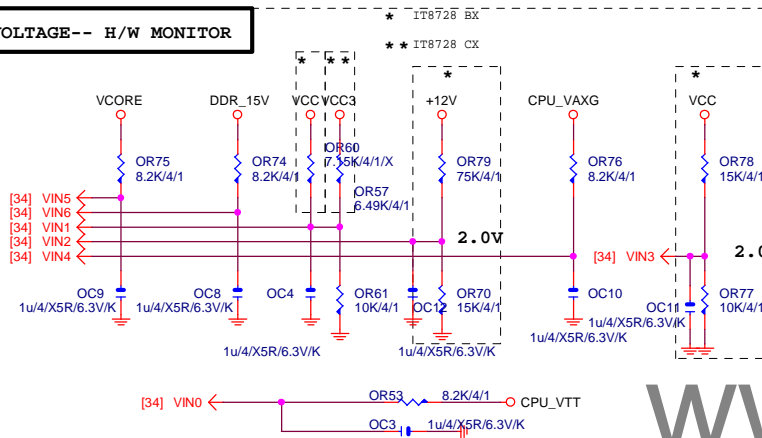
ATX POWER CONNECTOR



TEMP H/W MONITOR

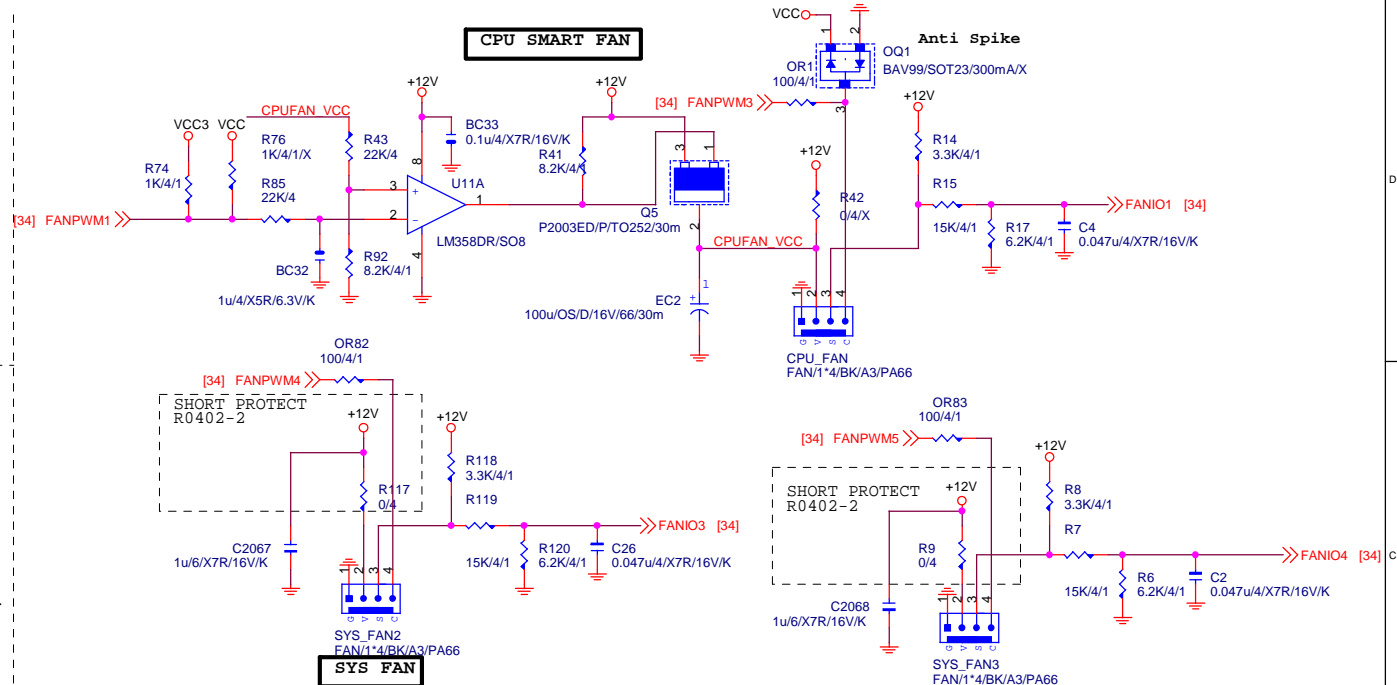


VOLTAGE-- H/W MONITOR

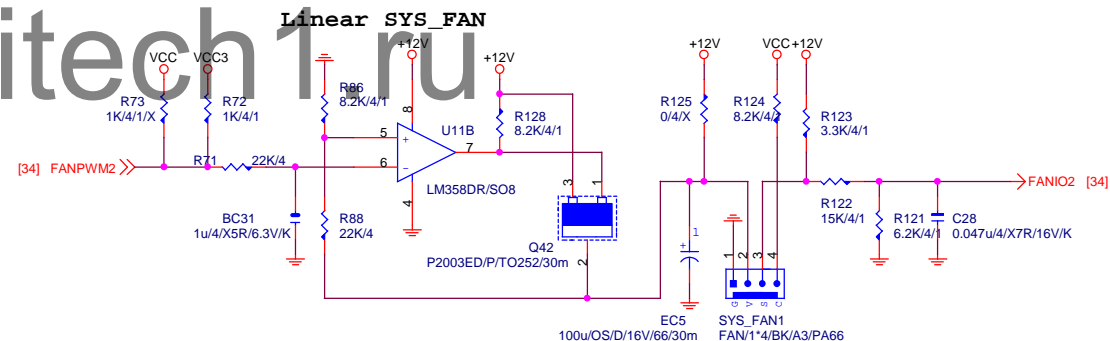


The division voltage of VIN2 & VIN3 must be around 2.9V

CPU SMART FAN

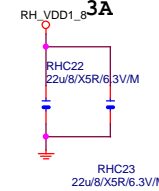
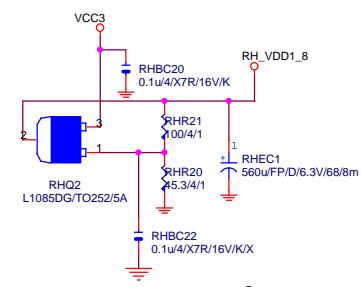
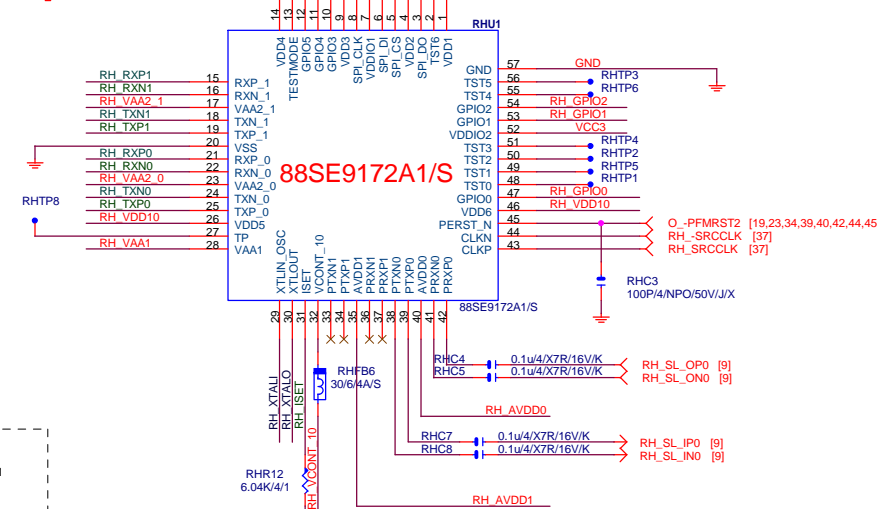
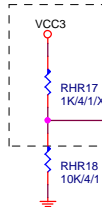
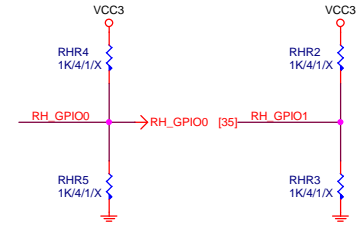
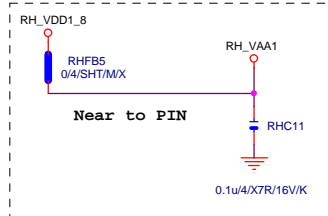
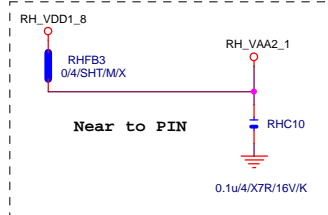
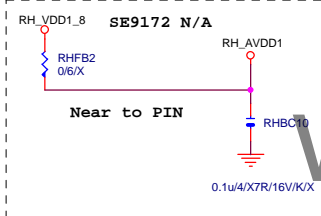
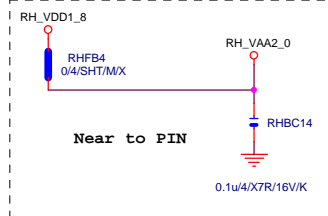
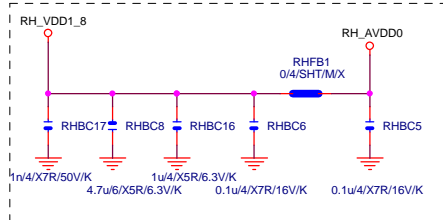
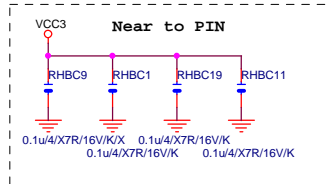
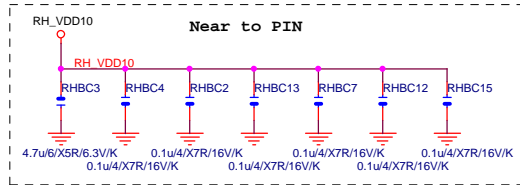


SYS FAN

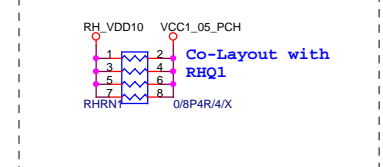
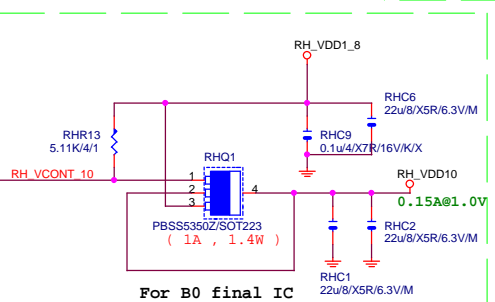
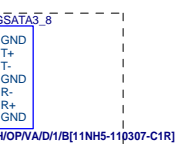
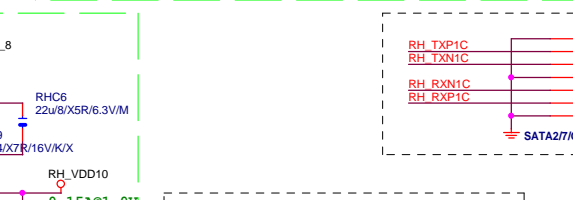
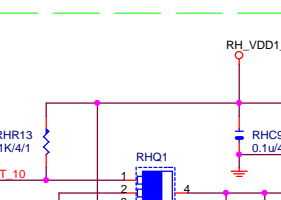
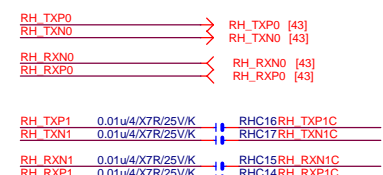
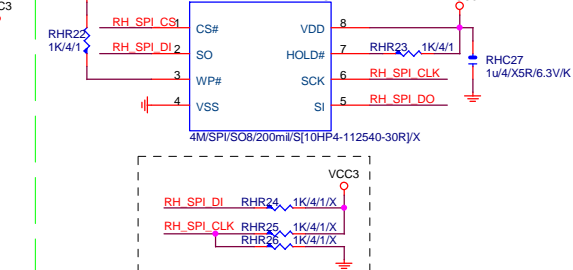
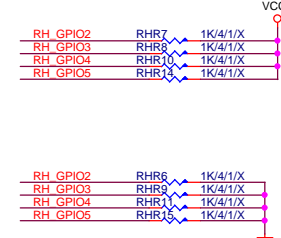


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Title			
HWM,KB/MS, FAN CTRL			
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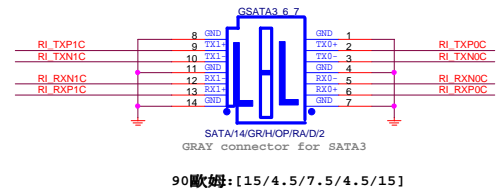
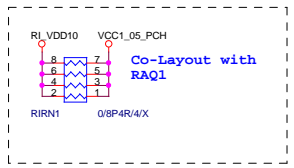
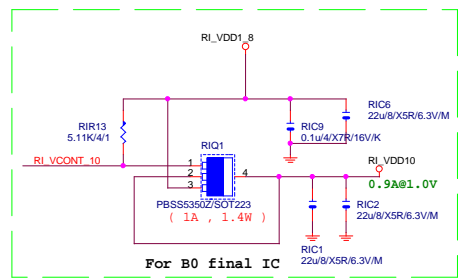
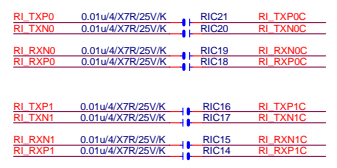
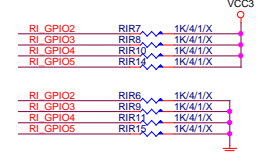
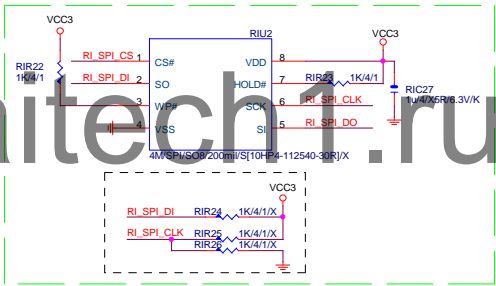
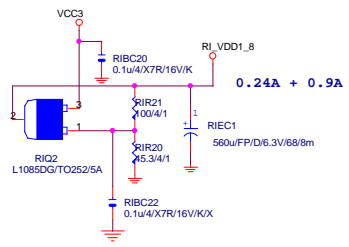
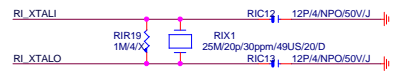
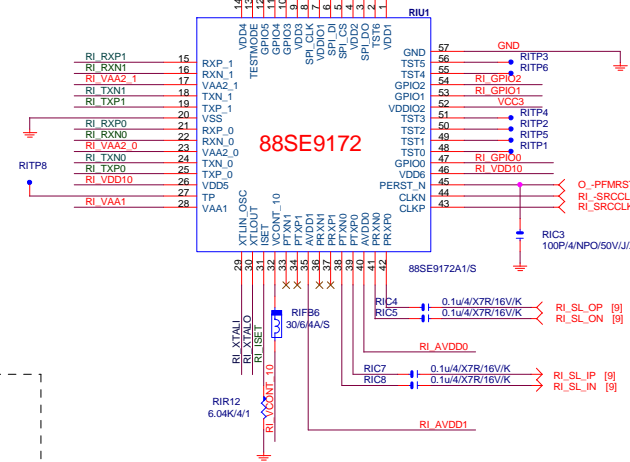
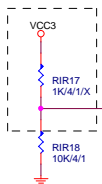
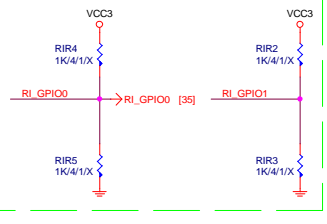
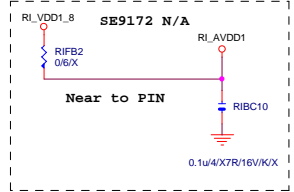
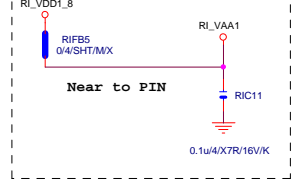
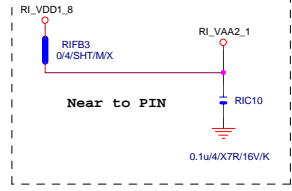
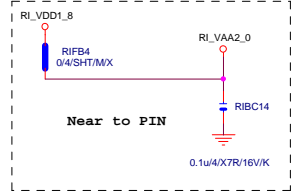
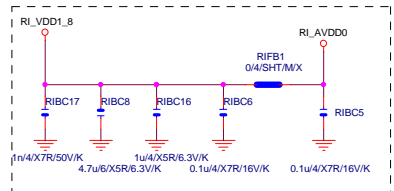
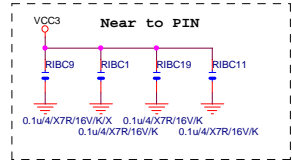
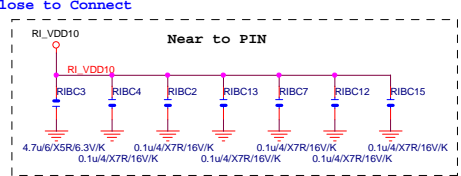


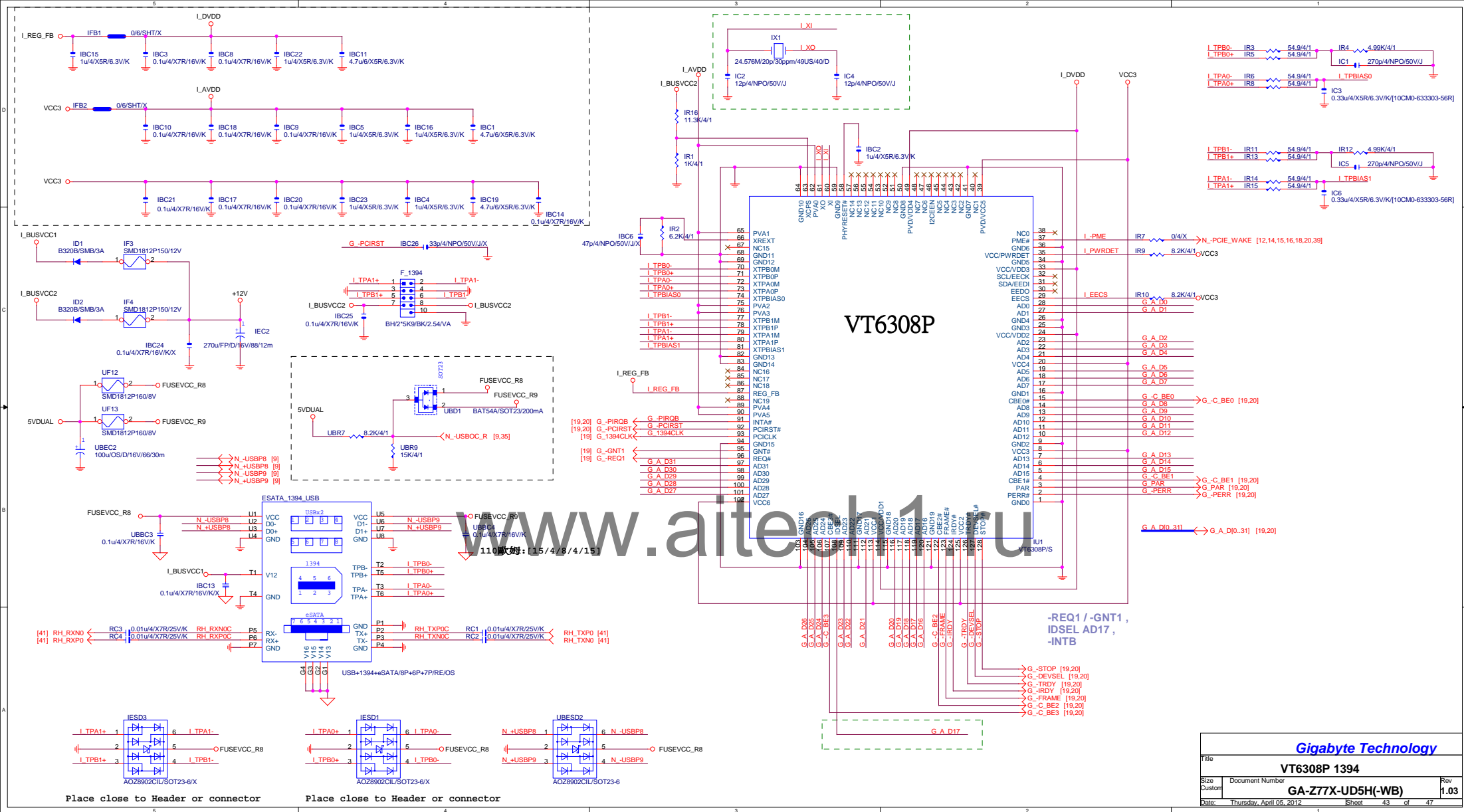
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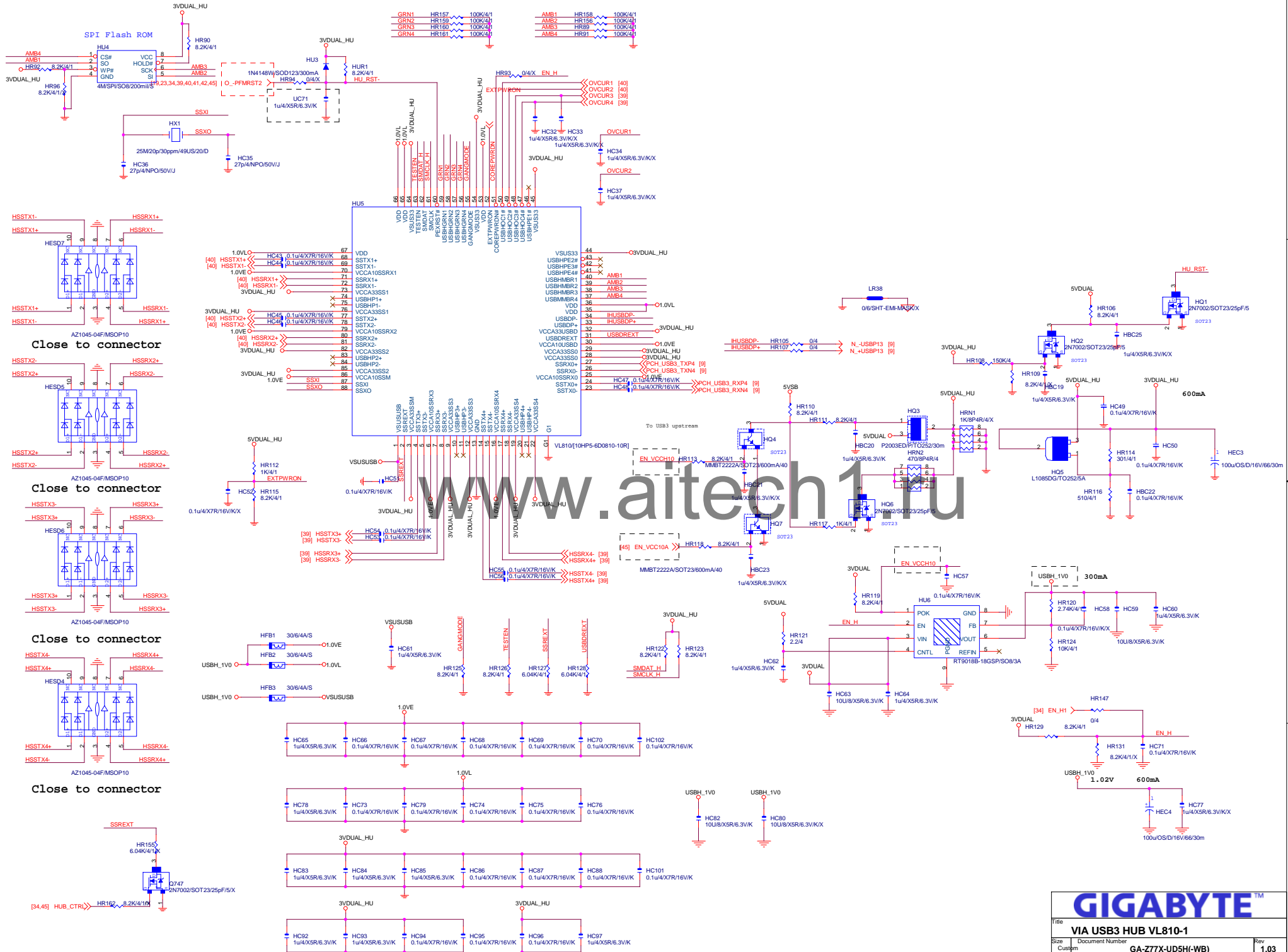


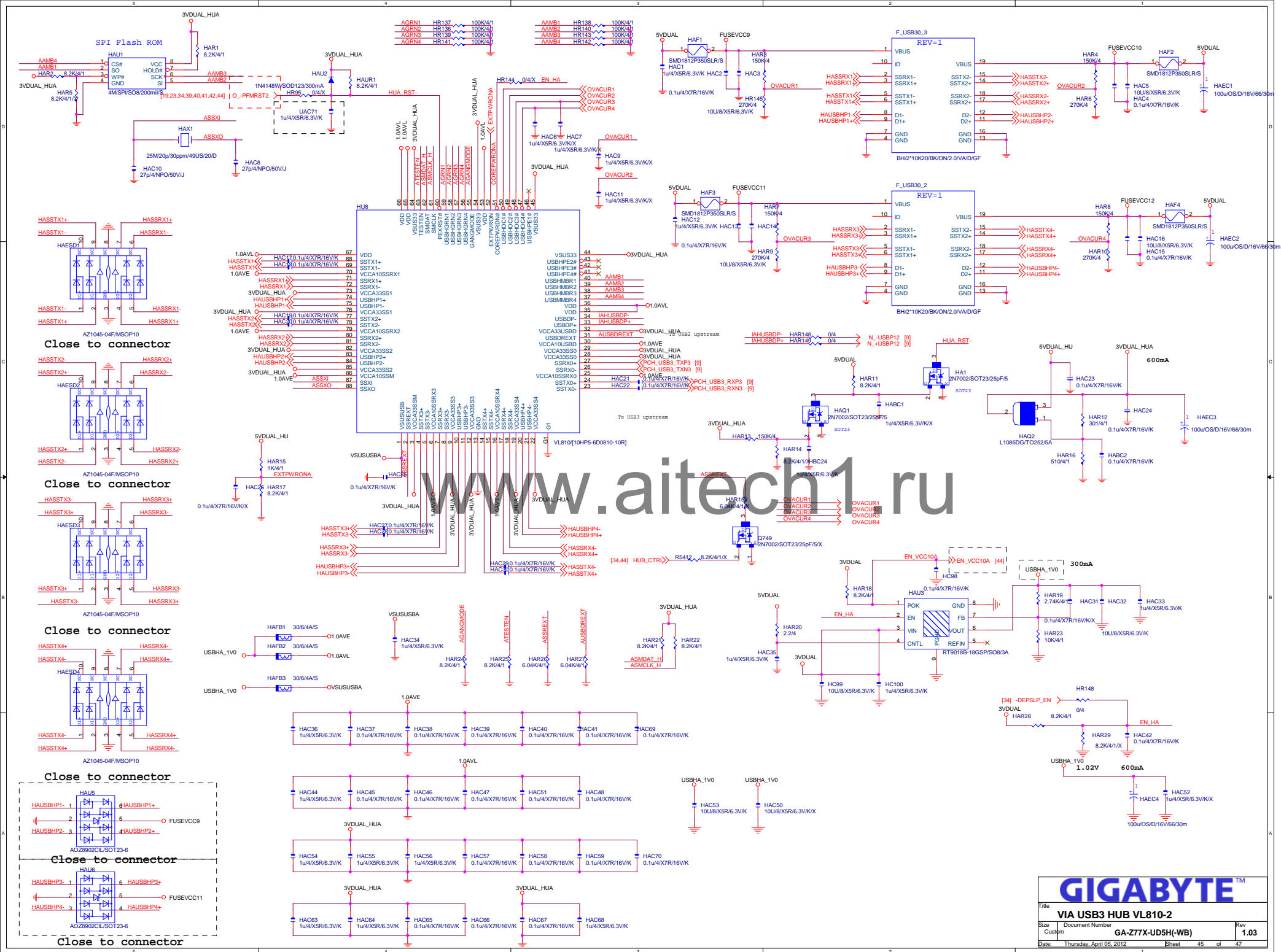
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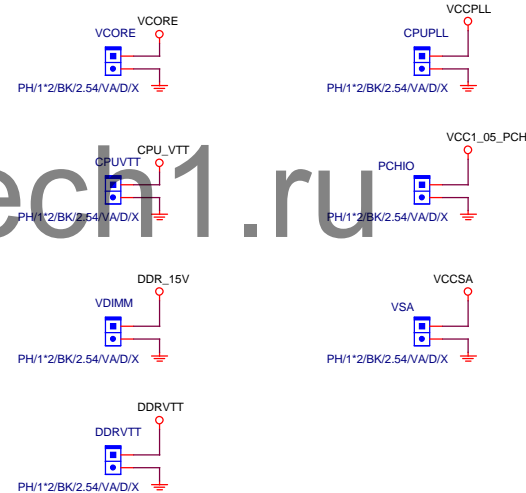
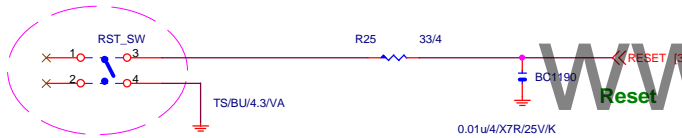
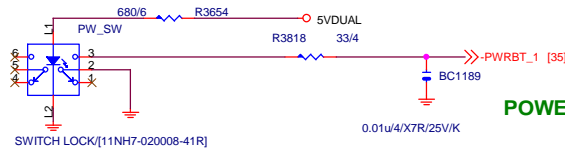
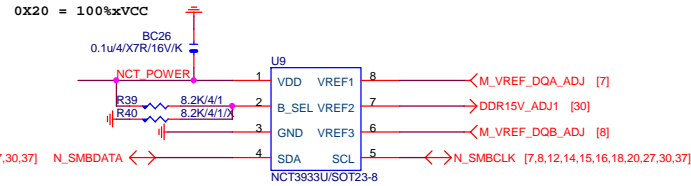
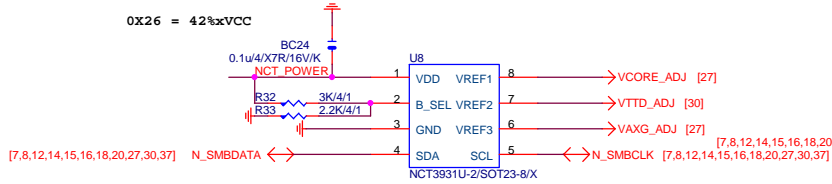
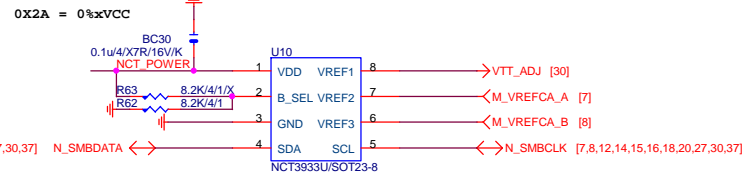
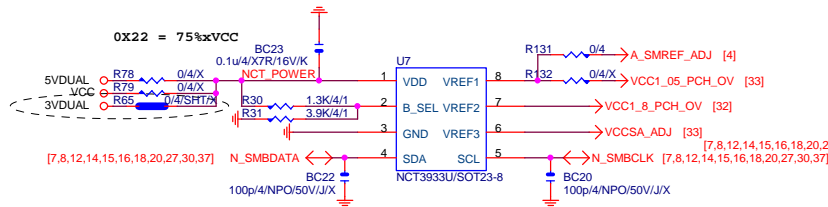
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Title		
Marvell 9220 SATA 3.0		
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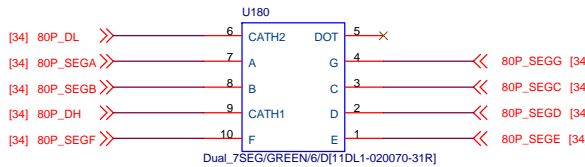
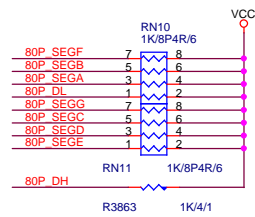




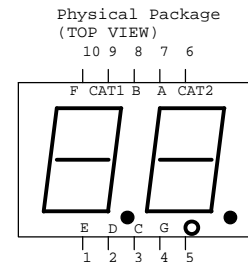




80 PORT



COMMON CATHODE

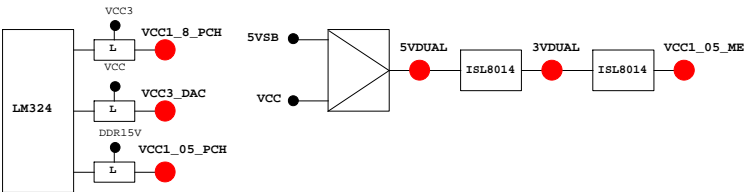


PCH GPIO LIST TABLE				
PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI -PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI -PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE OC5#	N/A
GP10/OC6#	STBY		NATIVE OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE OC7#	N/A
GP15	STBY	L	GPO GPIO15	N/A
GP16	MAIN		GPI -SKT0CC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI VCC18_FCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI GPIO29	N/A
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE OC1#	N/A
GP41	STBY		NATIVE OC2#	N/A
GP42	STBY		NATIVE OC3#	N/A
GP43	STBY		NATIVE OC4#	N/A
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE -GNT1	N/A
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE -GNT2	N/A
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE -GNT3	N/A
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE -SUSTAT	N/A
GP62	STBY	L	NATIVE SUSCLK	N/A
GP63	STBY	L	NATIVE GPIO63	N/A
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL

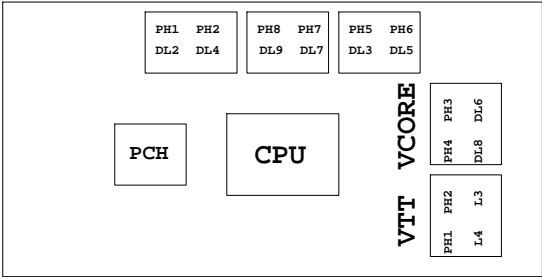
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRMST1	
PCIRST1#/GP12	-PWRMST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBD_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBD_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

散熱模組料號：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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